SPACE VECTOR PWM SIGNAL GENERATION FOR TWELVE-LEVEL INVERTER USING REFERENCE SIGNALS

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Abstract. A refined space vector modulation scheme for a twelve-level inverter system for dual-fed induction motor drive, using only the instantaneous sampled reference signals is presented in this paper. The dual-fed structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The twelve-level inversion is obtained by feeding the dual-fed induction motor with symmetrical four-level inverter from one end and symmetrical three-level inverter from other end. The proposed space vector pulse width modulation technique does not require the sector information and look-up tables to select the appropriate switching vectors. The inverter leg switching times are directly obtained from the instantaneous sampled reference signal amplitudes and centers the switching times for the middle space vectors in a sampling time interval, as in the case of conventional space vector pulse width modulation.

Keywords: dual-fed induction motor, middle space vectors, space vector PWM, twelve-level inverter

1. Introduction

The two most widely used pulse width modulation (PWM) schemes for multilevel inverters are the carrier-based sine-triangle PWM (SPWM) scheme and the space vector PWM (SVPWM) scheme. The SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [1, 2]. The maximum peak of the fundamental component in the output voltage obtained with space vector modulation is 15% greater than with the sine-triangle modulation scheme [2-5]. But the conventional SVPWM scheme requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors [3, 4]. This makes the implementation of the SVPWM scheme quite complicated. It has been shown that, for two-level inverters, a SVPWM like performance can be obtained with a SPWM scheme by adding a common mode voltage of suitable magnitude, to the sinusoidal reference signals [4, 5]. A simplified method, to determine the correct offset times for centering the time durations of the middle space vectors, in a sampling time interval, is presented [8], for the two-level inverter.

The SPWM scheme, when applied to multilevel inverters, uses a number of level-shifted carrier signals to compare with the sinusoidal reference signals [9, 19, 20]. The SVPWM for multilevel inverters [10, 11] involves mapping of the outer sectors to an inner sub-hexagon sector, will be very complex, as a large number of sectors and inverter vectors are involved.

A modulation scheme is presented in [12], where a fixed common mode voltage is added to the reference signal throughout the modulation range. It has been shown [13] that this common mode addition will not result in a SVPWM-like performance, as it will not centre the middle space vectors in a sampling interval. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters [13]. A SVPWM scheme based on the above principle has been presented [14], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes. But it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented [15], where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM. The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the sinusoidal reference signal amplitudes. A SVPWM scheme is presented [18], where the switching time for the inverter legs is directly determined from sampled sinusoidal reference signal amplitudes for five-level inverter where two three-level inverters feed the dual-fed induction motor. A carrier based SPWM scheme is presented [20], for twelve-level inverter.

The objective of this paper is to present an implementation scheme for PWM signal generation for twelve-level inverter system for dual-fed induction motor, similar to the SVPWM scheme. In the proposed scheme, the dual-fed induction motor is fed with symmetrical four-level inverter from one end and symmetrical three-level inverter from other end. The PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the sinusoidal reference signals. A simple way of adding an offset voltage to the sinusoidal reference signals, to generate the SVPWM pattern, from only the sampled amplitudes of sinusoidal reference signals, is explained. The proposed SVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme presented in [14]. Also, the algorithm does not require either sector identification or look-up tables for switching vector determination as are required in the conventional multilevel SVPWM schemes [10, 11]. Thus the scheme is computationally efficient when compared to conventional multilevel SVPWM schemes, making it superior for real-time implementation.

2. Twelve-level inverter scheme for the dual-fed induction motor

The power circuit of the proposed drive is shown in Figure 1. A symmetrical four-level inverter, Inverter-A and a symmetrical three-level inverter, Inverter-B feed the dual-fed induction motor. The inverter-A is composed of three conventional two-level inverters INV-1, INV-2, and INV-3 in cascade. The Inverter-B is composed of two conventional two-level inverters INV-4 and INV-5 in cascade. The DC link voltages of INV-1, INV-2, INV-3, INV-4, and INV-5 are (3/11)Edc, (3/11)Edc, (3/11)Edc, (1/11)Edc, and (1/11)Edc respectively, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive.

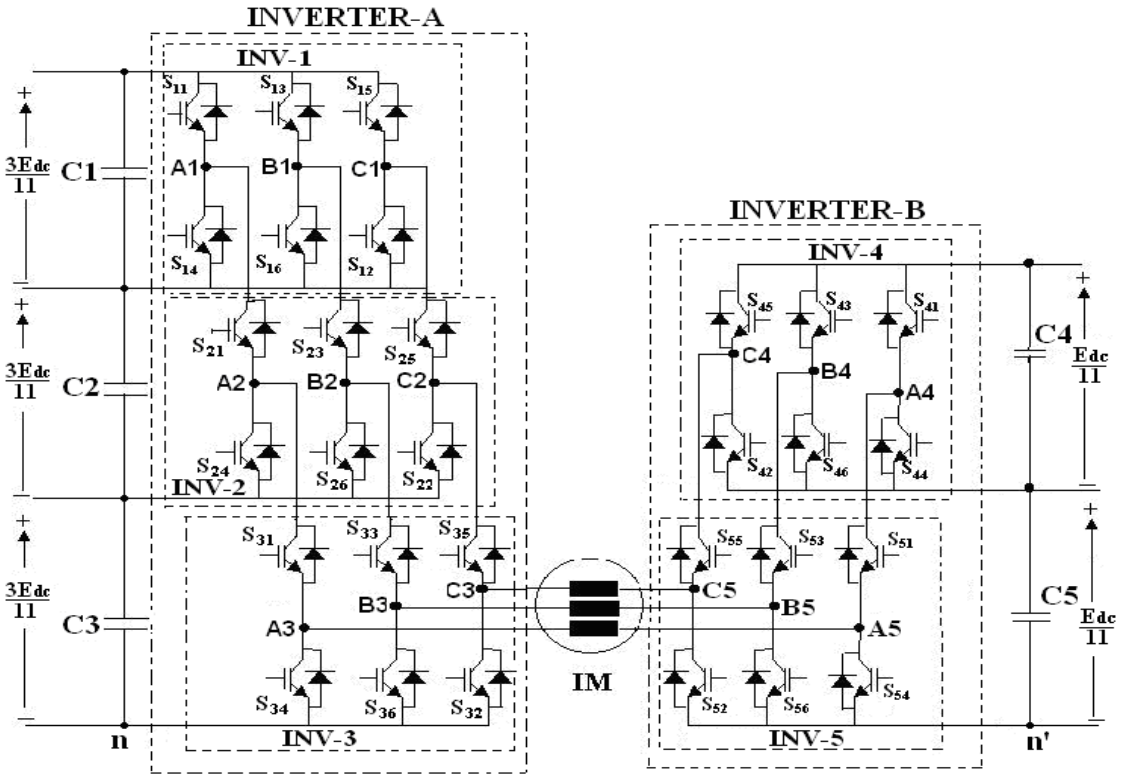


Figure 1. Schematic circuit diagram of the proposed 12-level inverter drive scheme

The leg voltage E_{A3n} of phase-A attains a voltage of (3/11)Edc if the switches S_{31} and S_{24} are turned on (Fig. 1). The leg voltage E_{A3n} of phase-A attains a voltage of (6/11)Edc if the switches S_{31}, S_{21}, and S_{14} are turned on. The leg voltage E_{A3n} of phase-A attains a voltage of (9/11)Edc if the switches S_{31}, S_{21}, and S_{11} are turned on. The leg voltage E_{A3n} of phase-A attains a voltage of zero volts if the switch S_{34} is turned on. Thus the leg voltage E_{A3n} attains four voltages of 0, (3/11)Edc, (6/11)Edc, and (9/11)Edc, which is basic characteristic of a 4-level inverter. Similarly the leg voltages E_{B3n} and E_{C3n} of phase-B and phase-C attain the four voltages of 0, (3/11)Edc, (6/11)Edc, and (9/11)Edc.

The leg voltage $E_{A5n'}$ of phase-A attains a voltage of (1/11)Edc if the switches S_{51} and S_{44} are turned on. The leg voltage $E_{A5n'}$ of phase-A attains a voltage of (2/11)Edc if the switches S_{51} and S_{41} are turned on. The leg voltage $E_{A5n'}$ of phase-A attains a voltage of zero volts if the switch S_{54} is turned on. Thus the leg voltage $E_{A5n'}$ attains three voltages of 0, (1/11)Edc, and (2/11)Edc, which is basic characteristic of a 3-level inverter. Similarly the leg voltages $E_{B5n'}$ and $E_{C5n'}$ of phase-B and phase-C attain the three voltages of 0, (1/11)Edc, and (2/11)Edc.

Thus, one end of dual-fed induction motor may be connected to a DC link voltage of either zero or (3/11)Edc or (6/11)Edc or (9/11)Edc and other end may be connected to a DC link voltage of either zero or (1/11)Edc or (2/11)Edc. When both the inverters, Inverter-A and Inverter-B drive the induction motor from both ends, twelve different levels are attained by each phase of the induction motor. The twelve levels generated for phase-A are shown in Table 1. Similarly the twelve levels of phase-B and phase-C can also be determined.

Table 1. The twelve levels realized in the phase-A winding

Leg-voltage of phase-A, E_{A3n}	Leg-voltage of phase A, $E_{A5n'}$	Motor phase voltage $E_{A3A5} = E_{A3n} - E_{A5n'}$	Level
0	(2/11) Edc	-(2/11) Edc	Level 1
0	(1/11) Edc	-(1/11) Edc	Level 2
0	0	0	Level 3
(3/11) Edc	(2/11) Edc	(1/11) Edc	Level 4
(3/11) Edc	(1/11) Edc	(2/11) Edc	Level 5
(3/11) Edc	0	(3/11) Edc	Level 6
(6/11) Edc	(2/11) Edc	(4/11) Edc	Level 7
(6/11) Edc	(1/11) Edc	(5/11) Edc	Level 8
(6/11) Edc	0	(6/11) Edc	Level 9
(9/11) Edc	(2/11) Edc	(7/11) Edc	Level 10
(9/11) Edc	(1/11) Edc	(8/11) Edc	Level 11
(9/11) Edc	0	(9/11) Edc	Level 12

3. Proposed SVPWM in Linear Modulation Range

For two-level inverters, in the SPWM scheme, each sinusoidal reference signal is compared with the triangular carrier signal and the individual phase voltages are generated [1]. To attain the maximum possible peak amplitude of the fundamental phase voltage, a common offset voltage, Eoffset1 is added to the sinusoidal reference signals [5, 12], where the magnitude of Eoffset1 is given by

$$Eoffset1 = -(E\max + E\min)/2 \quad (1)$$

Where Emax and Emin are the maximum and minimum magnitudes of the three sampled sinusoidal reference signals respectively, in a sampling time interval. The addition of Eoffset1, results in the active space vectors being centered, making the SPWM scheme equivalent to the SVPWM scheme [3]. In a sampling time interval, the sinusoidal reference signal which has lowest magnitude crosses the triangular carrier signal first, and causes the first transition in the inverter switching state and the sinusoidal reference signal, which has the maximum magnitude, crosses the triangular carrier signal last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [5, 13].

For twelve-level inverter, the modified sinusoidal reference signals (E^*_{AN}, E^*_{BN}, and E^*_{CN}) after addition of offset voltage Eoffset1, are shown in Figure 2 along with eleven triangular carrier signals T1 to T11. Each time a sinusoidal reference signal crosses the triangular carrier signal, it causes a change in the inverter switching state. The changes in phase voltage and their time intervals are shown in Figure 3 in a sampling time interval Ts. The sampling time interval Ts can be split into four time intervals t_{01}, t_1, t_2, and t_{02}. The time intervals t_{01} and t_{02} are the time durations for the start and end inverter space vectors respectively and the time intervals t_1 and t_2 are the time durations for the middle inverter space vectors (active space vectors), in a sampling time interval Ts. It should be observed from Figure 3 that the middle space vectors are not centered in a sampling time interval Ts. Because of the level-shifted eleven triangular carrier signals (Figure 2), the first crossing and the last crossing of the sinusoidal reference signal cannot always be the minimum and the maximum magnitude of the three sampled sinusoidal reference signals, in a sampling time interval. Thus the offset voltage, Eoffset1 is not sufficient to center the

middle inverter space vectors, in a multilevel PWM system (Figure 3). Hence an additional offset (offset2) has to be added to the sinusoidal reference signals of Figure 2, so that the middle inverter space vectors can be centered in a sampling time interval, same as a two-level SVPWM system [3].

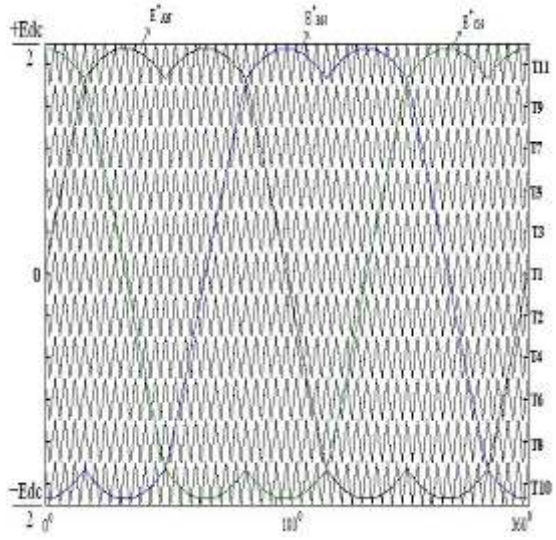


Figure 2. Modified sinusoidal reference signals and triangular carrier signals for a twelve-level PWM scheme

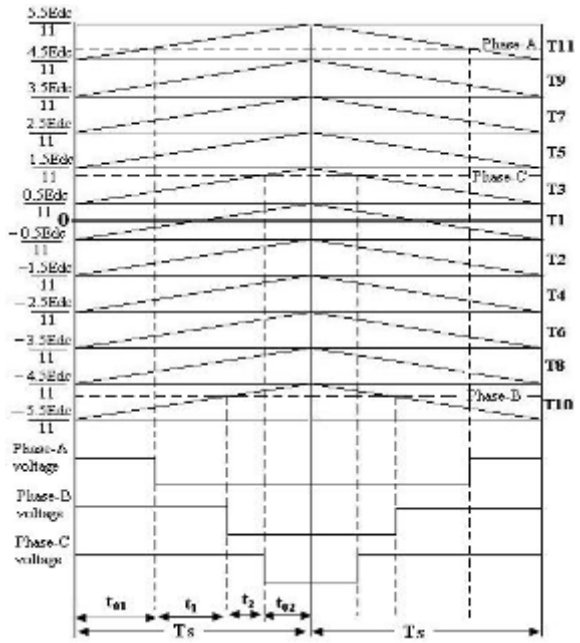


Figure 3. Inverter switching vectors and their switching time durations during sampling time interval

4. Determination of the offset voltage for a twelve-level inverter

The time interval, at which the A-phase sinusoidal reference signal, E^*_{AN} crosses the triangular carrier signal, is termed as Ta-cross (Figure 4). Similarly, the time intervals, when the B-phase and C-phase sinusoidal reference signals, E^*_{BN} and E^*_{CN} cross the triangular carrier signals, are termed as Tb-cross and Tc-cross respectively.

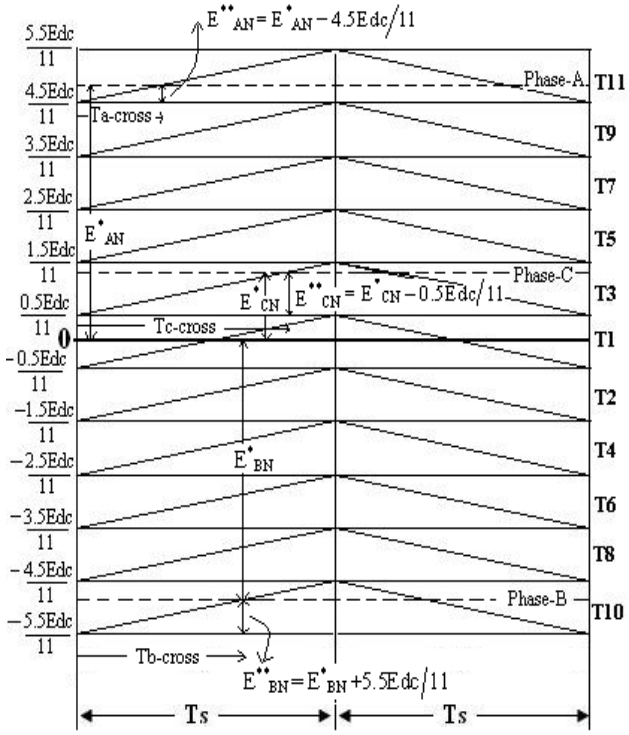


Figure 4. Determination of the Ta-cross, Tb-cross and Tc-cross during sampling interval Ts

Figure 4 shows a sampling time interval when the A-phase sinusoidal reference signal is in the triangular carrier region T11 while the B-phase and C-phase sinusoidal reference signals are in carrier region T10 and T3 respectively. As shown in Figure 4, the time interval, Ta-cross, at which the A-phase sinusoidal reference signal crosses the triangular carrier signal, is directly proportional to the phase voltage amplitude, (E^*_{AN} − 4.5Edc /11). And Tb-cross and Tc-cross are proportional to (E^*_{BN} + 5.5Edc /11) and (E^*_{CN} − 0.5Edc /11) respectively. Therefore

$$Ta-cross = (E^*_{AN} - 4.5Edc/11)\left(\frac{Ts}{Edc/11}\right) = T^*as - 4.5Ts$$

$$Tb-cross = (E^*_{BN} + 5.5Edc/11)\left(\frac{Ts}{Edc/11}\right) = T^*bs + 5.5Ts \quad (2)$$

$$Tc-cross = (E^*_{CN} - 0.5Edc/11)\left(\frac{Ts}{Edc/11}\right) = T^*cs - 0.5Ts$$

Where T^*as, T^*bs and T^*cs are the time equivalents of the voltage magnitudes. The proportionality between the time equivalents and corresponding voltage magnitudes is defined as follows [8]:

$$(Edc/11)/Ts = E^*_{AN}/T^*as$$
$$(Edc/11)/Ts = E^*_{BN}/T^*bs$$
$$(Edc/11)/Ts = E^*_{CN}/T^*cs \quad (3)$$
$$(Edc/11)/Ts = Eoffset1/Toffset1$$

The time interval, at which the sinusoidal reference signals cross the triangular carrier signals for the first time, is termed as Tfirst_cross. Similarly, the time intervals, at which the sinusoidal reference signals cross the triangular carrier signals for the second and third time, are termed as, Tsecond_cross and Tthird_cross respectively, in a sampling time interval Ts.

$$Tfirst\_cross = \min(Ta-cross, Tb-cross, Tc-cross)$$
$$T\,\text{second}\_cross = mid(Ta-cross, Tb-cross, Tc-cross) \quad (4)$$
$$Tthird\_cross = \max(Ta-cross, Tb-cross, Tc-cross)$$

The time intervals, Tfirst_cross, Tsecond_cross, and Tthird_cross, directly decide the switching times for the different inverter voltage vectors, forming a triangular sector, during one sampling time interval Ts. The time intervals for the start and end space vectors, are t_{01}= Tfirst_cross, t_{02}= (Ts − Tthird_cross), respectively (Figure 3). The middle space vectors are centered by adding a time offset, Toffset2 to Tfirst_cross, Tsecond_cross, and Tthird_cross. The time offset, Toffset2 is determined as follows. The time interval for the middle inverter space vectors, Tmiddle, is given by:

$$Tmiddle = Tthird\_cross - Tfirst\_cross \quad (5)$$

The time interval of the start and end space vector is

$$T_0 = Ts - Tmiddle \quad (6)$$

Thus the time interval of the start space vector is given by

$$T_0/2 = Tfirst\_cross + Toffset2\,.$$

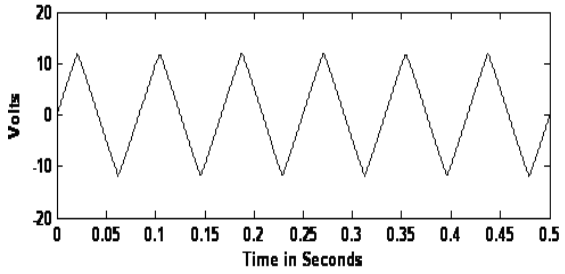
Therefore

$$Toffset2 = T_0/2 - Tfirst\_cross \quad (7)$$

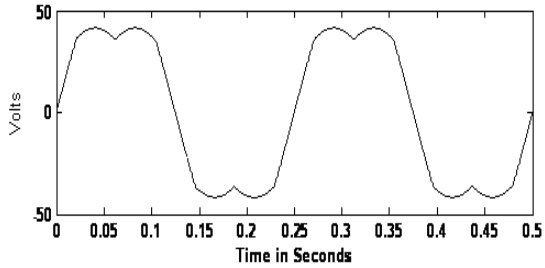
In this way, we can obtain offset voltages to be added for remaining samples during the time period of sinusoidal reference signal and for different modulation indices.

5. Simulation results and discussion

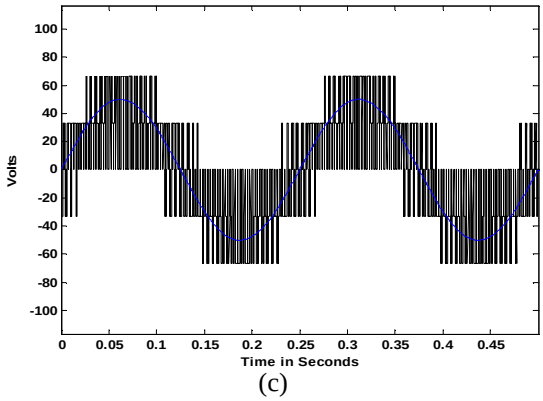
The proposed SVPWM scheme is simulated using MATLAB environment with open loop E/f control for different modulation indices. The respective DC link voltages are (3/11)Edc, (3/11)Edc, (3/11)Edc, (1/11)Edc, and (1/11)Edc for the INV-1, INV-2, INV-3, INV-4, and INV-5, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive. The speed reference is translated to the frequency and voltage commands maintaining E/f. The modified three reference sinusoidal signals which are added by the total offset voltage to make SPWM scheme equivalent to the SVPWM scheme, are simultaneously compared with the triangular carrier set. A DC link voltage (Edc) of 1100 volts is assumed for simulation studies. Figure 5a shows the total offset voltage to be added to sinusoidal reference signals to make SPWM equivalent to the SVPWM in the lowest speed range which corresponds to two-level mode when modulation index is 0.07. Figure 5b shows the A-phase sinusoidal reference signal after offset voltage is added and Figure 5c shows the motor phase voltage (E_{A3A5}).



(a)



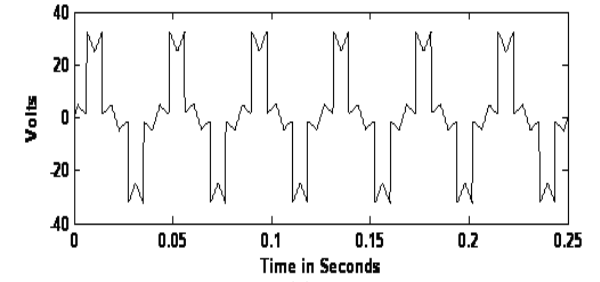
(b)



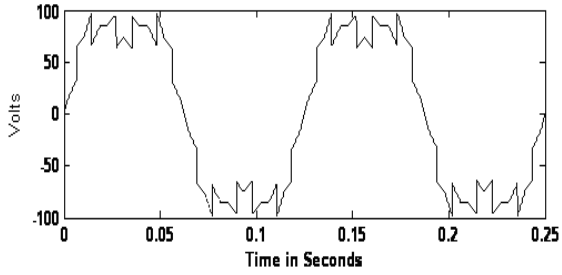
(c)

Figure 5. (a)The offset voltage to be added to sinusoidal reference signals (b). The A-phase sinusoidal reference signal after offset voltage is added (c) Motor phase voltage when M=0.07 (2-level operation)

Figure 6 to Figure 15 show the motor waveforms in the next speed ranges which corresponds to three-level mode to twelve-level mode when modulation indices are 0.14, 0.2, 0.3, 0.38, 0.4, 0.5, 0.6, 0.7, 0.77, and 0.85 respectively. It can be observed that the motor phase voltage during 12-level operation is very smooth and close to the sinusoid with lower harmonics.



(a)



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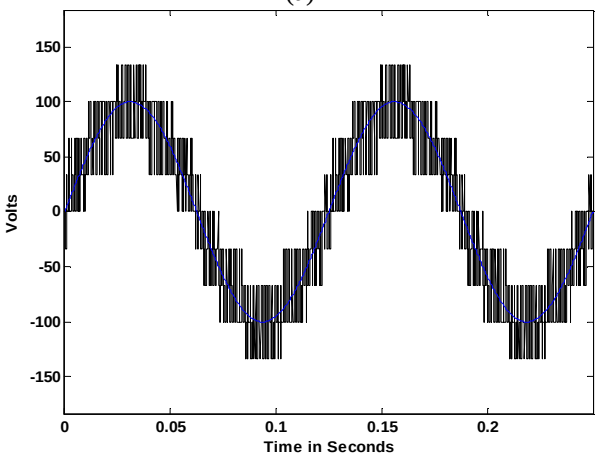
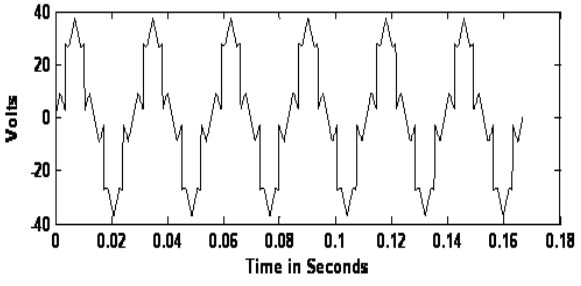
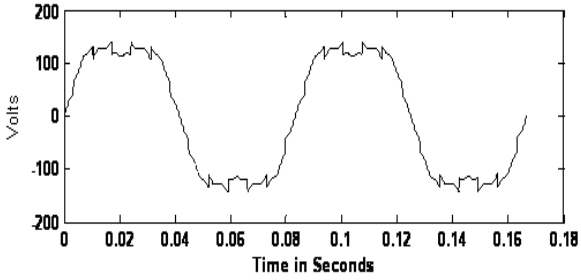


(c)

Figure 6.
(a) The offset voltage to be added to sinusoidal reference signals.
(b)The A-phase sinusoidal reference signal after offset voltage is added.
(c)Motor phase voltage when M=0.14 (3-level operation)



(a)



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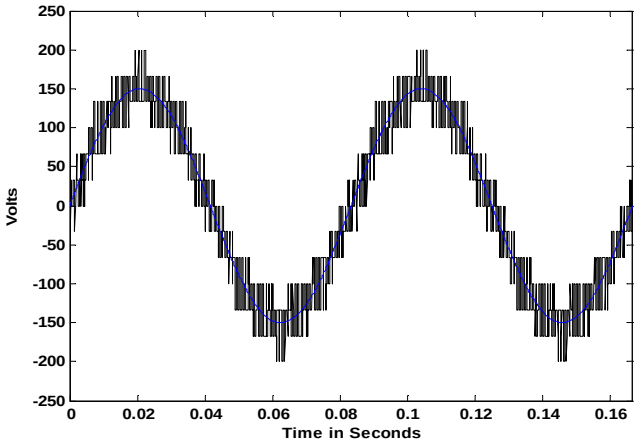
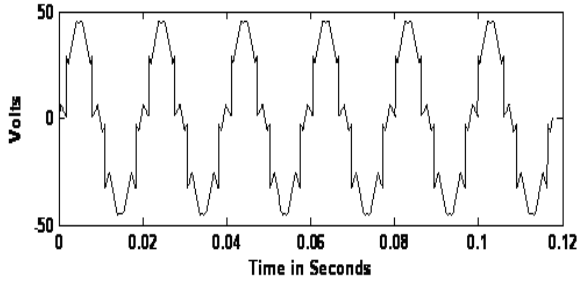
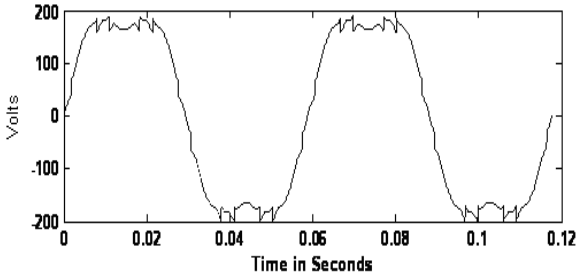


(c)

Figure 7.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.2 (4-level operation)



(a)



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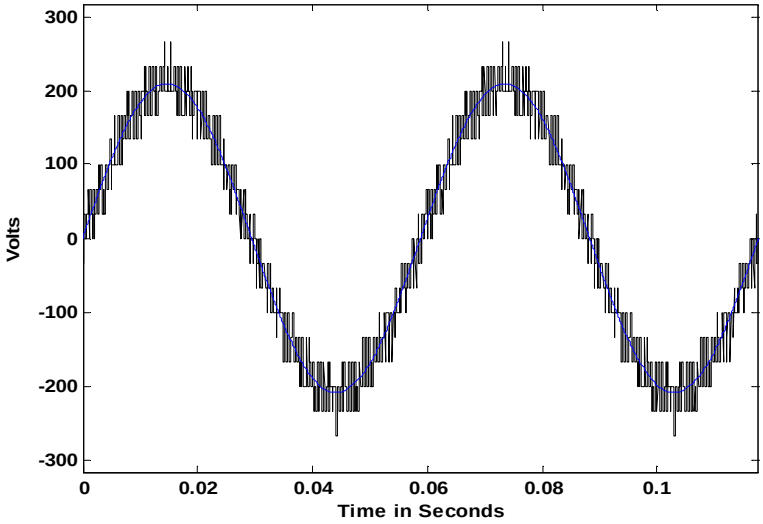
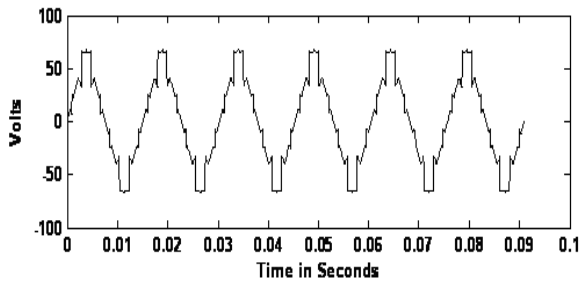
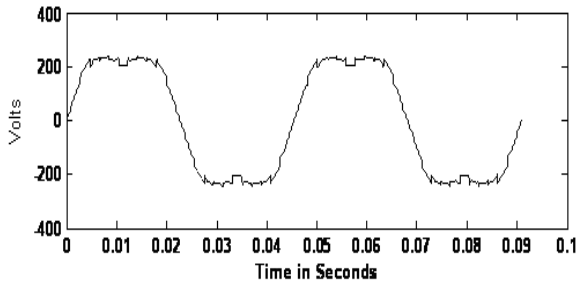


(c)

Figure 8.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.3 (5-level operation)



(a)



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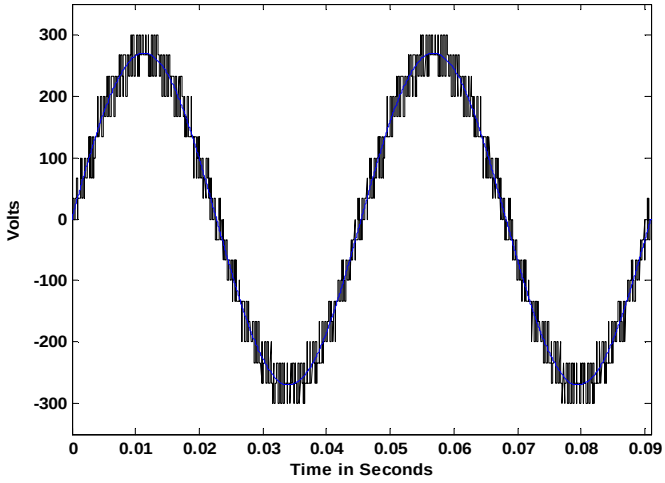


(c)

Figure 9.
(a)The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.38 (6-level operation)

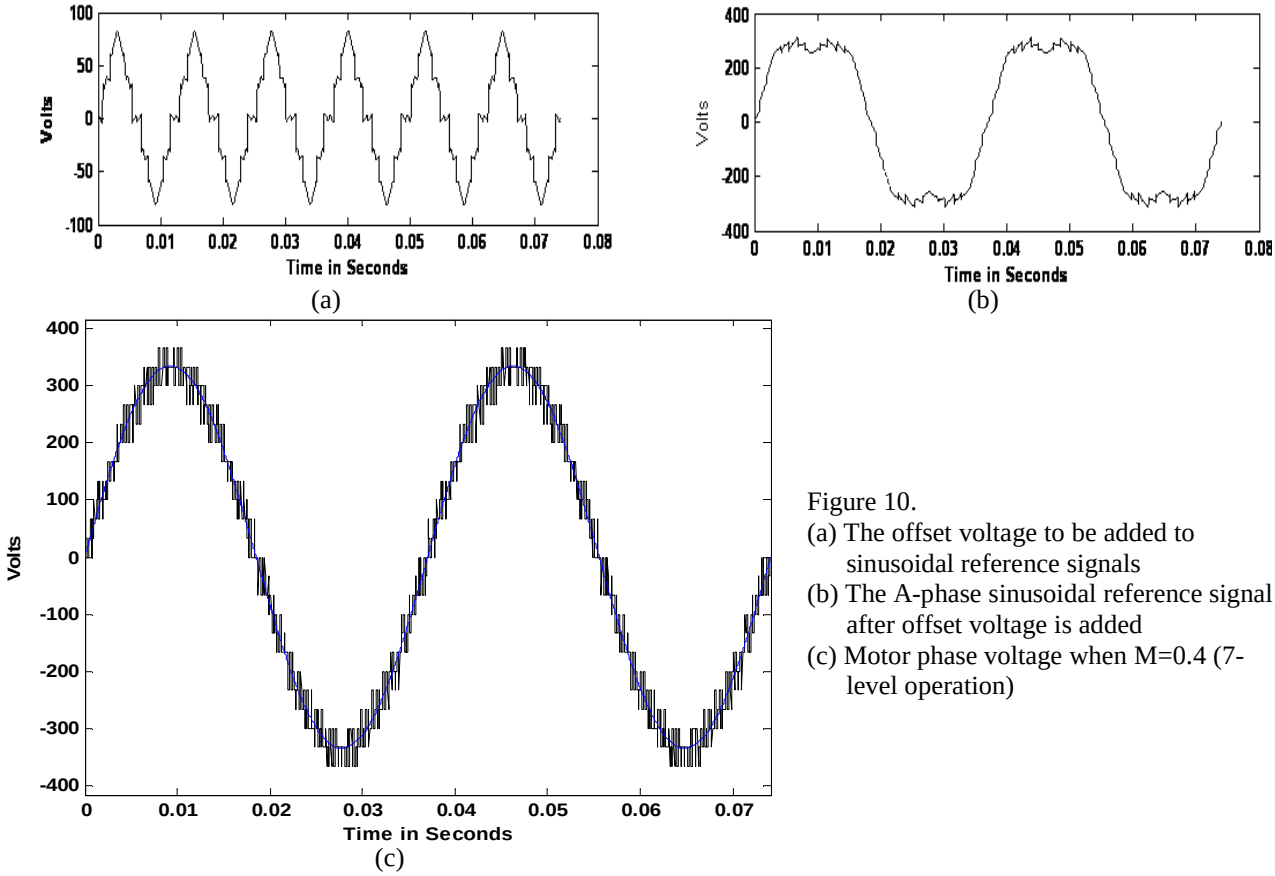


Figure 10.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.4 (7-level operation)

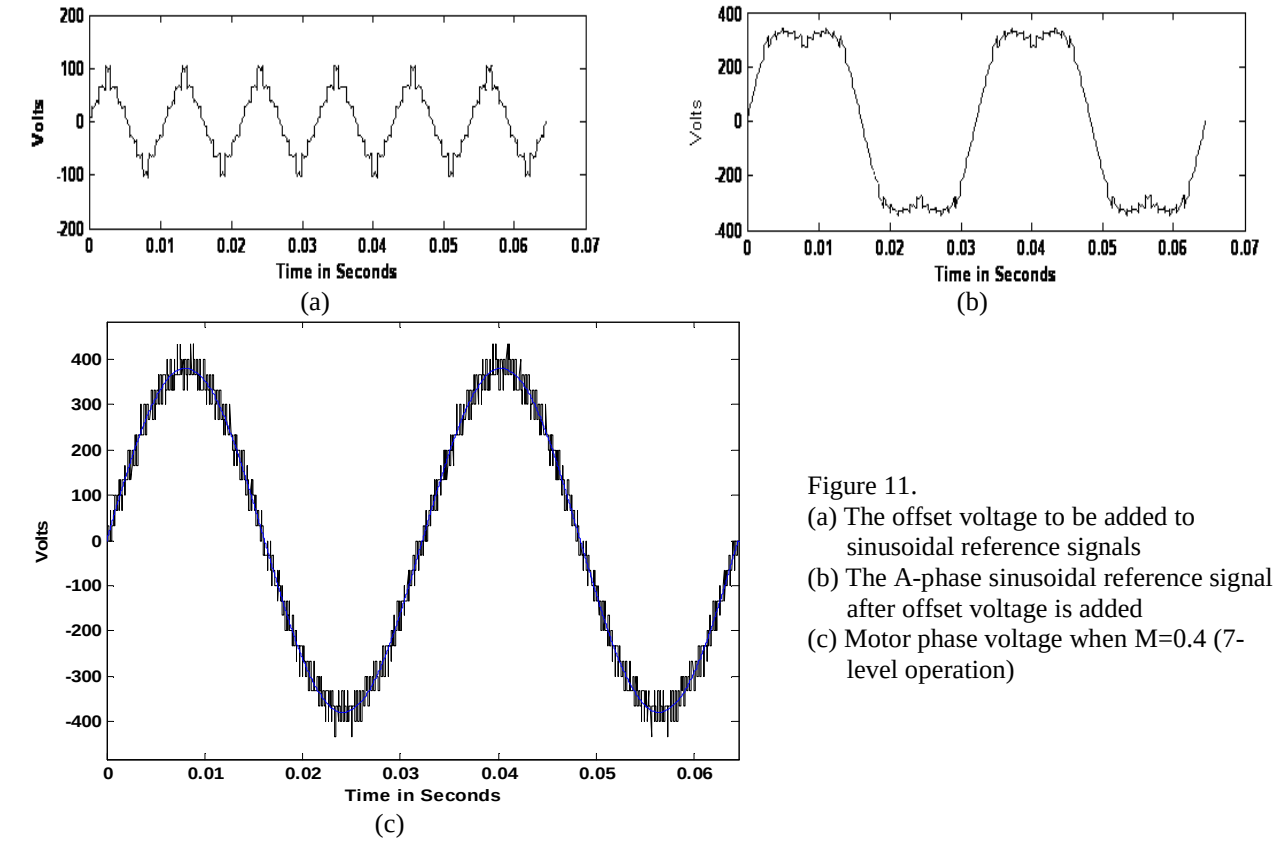
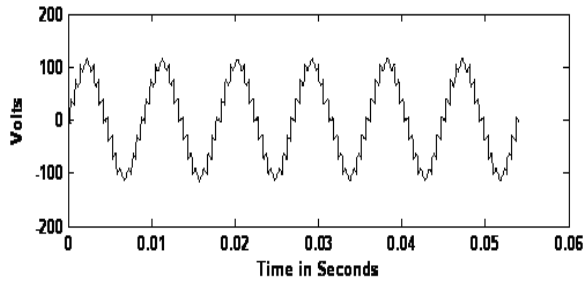
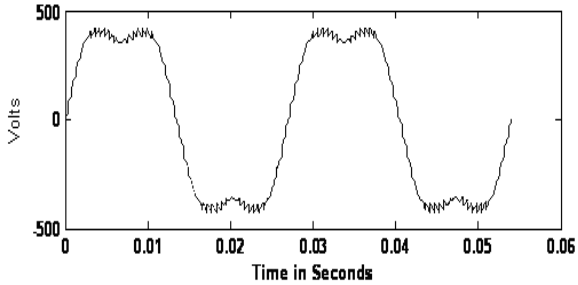


Figure 11.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.4 (7-level operation)



(a)



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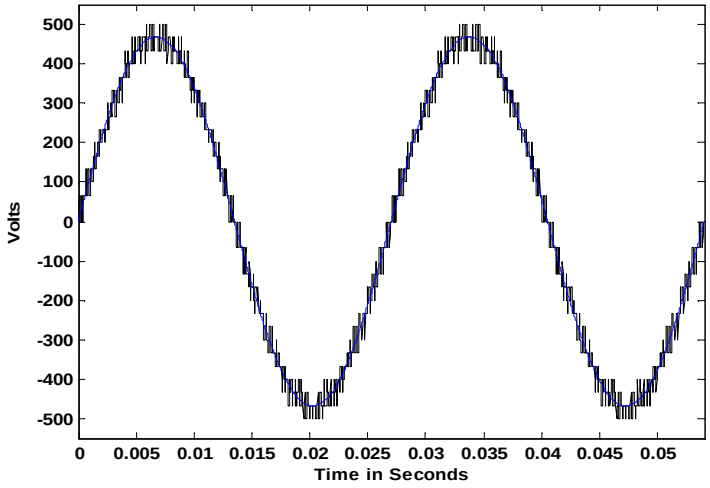
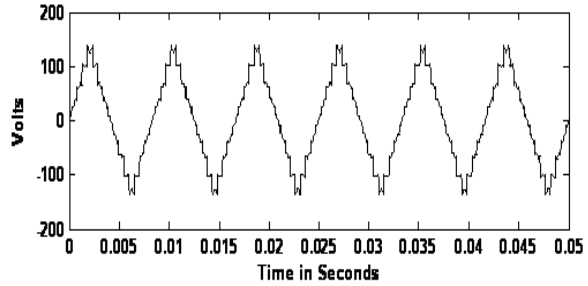
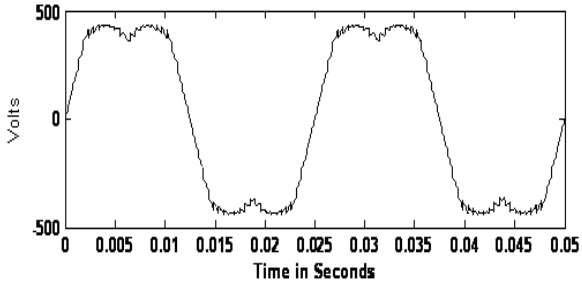


(c)

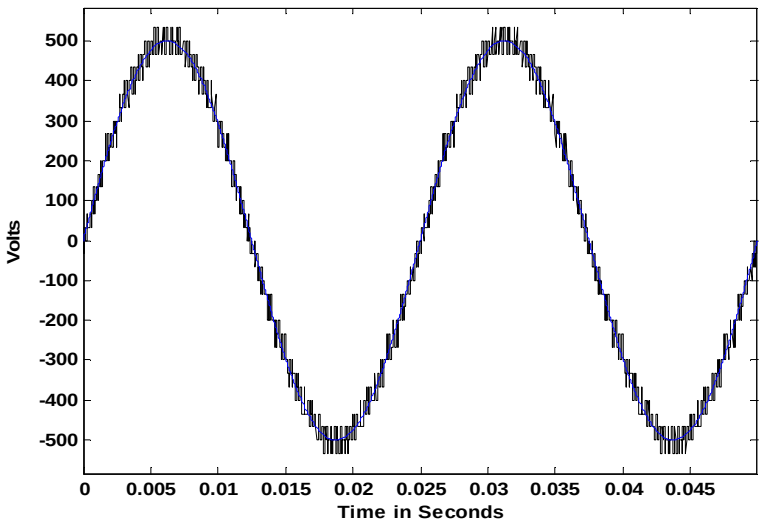
Figure 12.
(a)The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.6 (9-level operation)



(a)

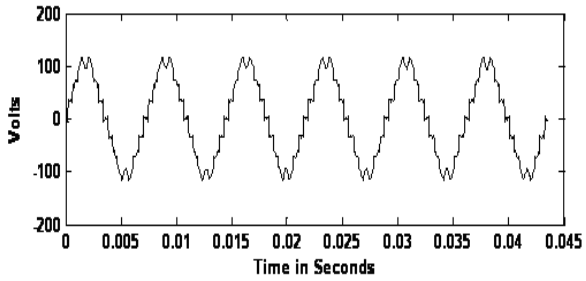


(b)

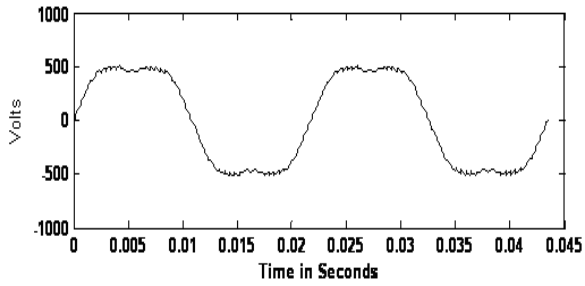


(c)

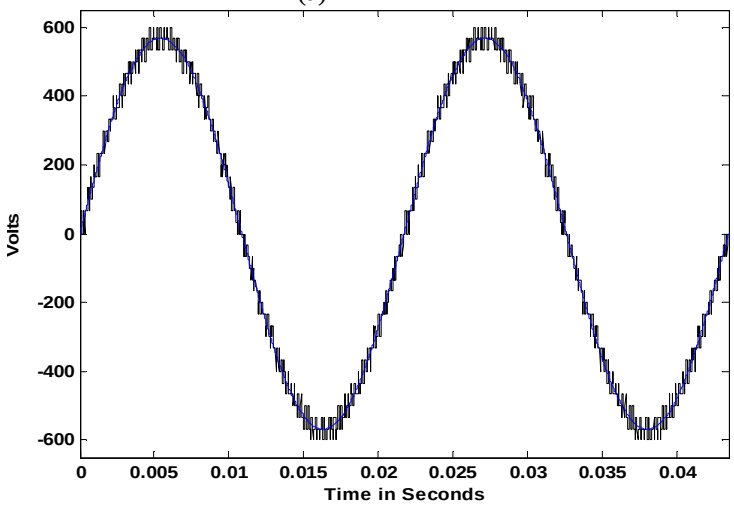
Figure 13.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.7 (10-level operation)



(a)

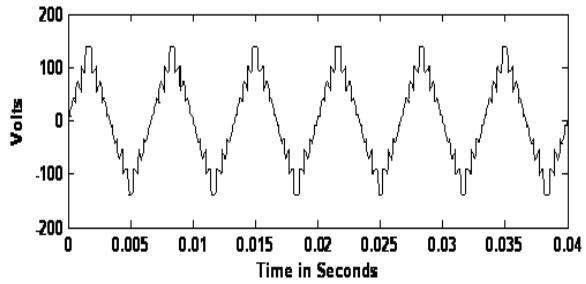


(b)

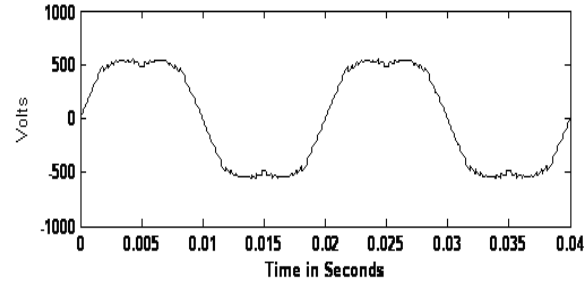


(c)

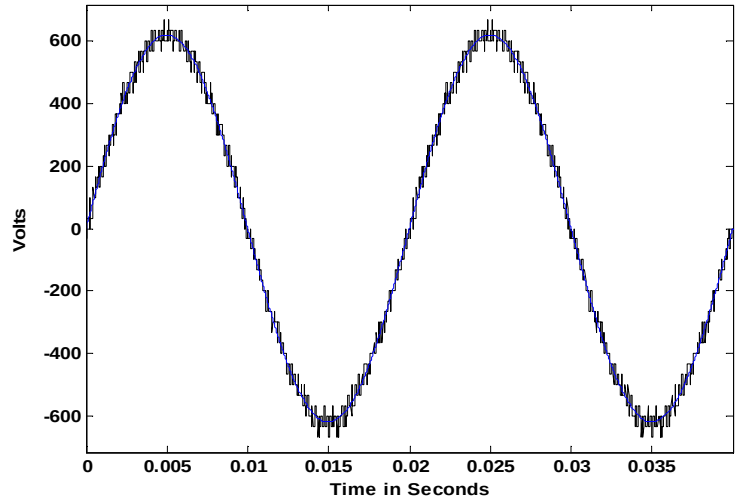
Figure 14.
(a) The offset voltage to be added to sinusoidal reference signals
(b)The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.77 (11-level operation)



(a)



(b)



(c)

Figure 15.
(a) The offset voltage to be added to sinusoidal reference signals
(b) The A-phase sinusoidal reference signal after offset voltage is added
(c) Motor phase voltage when M=0.85 (12-level operation)

6. Conclusion

A modulation scheme of SVPWM for twelve-level inverter system for dual-fed induction motor drive, where the induction motor is fed by symmetrical four-level inverter from one end and symmetrical three-level inverter from other end is presented. The symmetrical four-level inverter used is composed of three conventional two-level inverters with equal DC link voltage in cascade and the symmetrical three-level inverter used is composed of two conventional two-level inverters with equal DC link voltage in cascade. The centering of the middle inverter space vectors of the SVPWM is accomplished by the addition of an offset voltage signal to the sinusoidal reference signals, derived from the sampled amplitudes of the sinusoidal reference signals. The SVPWM technique, presented in this paper does not require any sector identification, as is required in conventional SVPWM schemes. The proposed scheme eliminates the use of look-up table approach to switch the appropriate space vector combination as in conventional SVPWM schemes. This reduces the computation time required to determine the switching times for inverter legs, making the algorithm suitable for real-time implementation.

References

1. Holtz, J. (1992) *Pulsewidth modulation–a survey*, IEEE Trans. Ind. Electron, Vol.30, No.5, (1992), p. 410–420, DOI: 10.1109/41.161472.
2. Zhou, K., Wang, D. (2002) *Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis*, IEEE Trans. Ind. Electron., Vol.49, No.1, (2002), p.186–196, DOI: 10.1109/41.982262.
3. van der Broeck, H.W., Skudelny, H.C., Stanke, G.V. (1988) *Analysis and realisation of a pulsewidth modulator based on voltage space vectors*, IEEE Trans. Ind. Appl., Vol.24, No.1, (1988), p. 142–150, DOI: 10.1109/28.87265.
4. Boys, J.T., Handley, P.G. (1990) *Harmonic analysis of space vector modulated PWM waveforms*, IEE Proc. Electr. Power Appl., Vol.137, No.4, (1990), p. 197–204.
5. Holmes, D.G. (1992) *The general relationship between regular sampled pulse width modulation and space vector modulation for hard switched converters*, Conf. Rec. IEEE Industry Applications Society (IAS) Annual Meeting, (1992), p. 1002–1009, DOI: 10.1109/IAS.1992.244437.
6. Holtz, J., Lotzkat, W., Khambadkone, A. (1993) *On continuous control of PWMinverters in over-modulation range including six-step mode*, IEEE Trans. Power Electron., Vol.8, No.4, (1993), p. 546–553, DOI: 10.1109/63.261026.
7. Lee, D., Lee, G. (1998) *A novel overmodulation technique for space vector PWM inverters*, IEEE Trans. Power Electron., Vol.13, No.6, (1998), p. 1144–1151, DOI: 10.1109/63.728341.
8. Kim, J., Sul, S. (1995) *A novel voltage modulation technique of the Space Vector PWM*, Proc. Int. Power Electronics Conf., Yokohama, Japan, (1995), p. 742–747
9. Carrara, G.,Gardella, S.G., Archesoni, M., Salutari, R., Sciutto, G. (1992) *A new multi-level PWM method: A theoretical analysis*, IEEE Trans. Power Electron., Vol.7, No.3, (1992), p. 497–505, DOI: 10.1109/63.145137.
10. Shivakumar, E.G., Gopakumar, K., Sinha, S.K., Pittet, A., Ranganathan, V.T. (2001) *Space vector PWM control of dual inverter fed open-end winding induction motor drive*, Proc. IEEE Applied Power Electronics Conf. (APEC), p.399–405, DOI: 10.1109/APEC.2001.911678.
11. Suh, J., Choi, C., Hyun, D. (1999) *A new simplified space vector PWM method for three-level inverter*, Proc. IEEE Applied Power Electronics Conf. (APEC), (1999), p. 515–520, DOI: 10.1109/APEC.1999.749730.
12. Baiju, M.R., Mohapatra, K.K., Somasekhar, V.T., Gopakumar, K., Umanand, L. (2003) *A five-level inverter voltage space phasor generation for an open-end winding induction motor drive*, IEE Proc. Electr. Power Appl., Vol.150, No.5, (2003), p. 531–538, DOI: 10.1049/ip-epa:20030659.
13. Wang, F. (2000) *Sine-triangle versus space vector modulation for threelevel PWM voltage source inverters*, Proc. IEEE-IAS Annual Meeting, Rome, (2000), p. 2482–2488, DOI: 10.1109/IAS.2000.883171.
14. Baiju, M.R., Gopakumar, K., Somasekhar, V.T., Mohapatra, K.K., Umanand, L. (2003) *A space vector based PWMmethod using only the instantaneous amplitudes of reference phase voltages for three-level inverters* EPE J., Vol.13, No.2, (2003), p. 35–45, ISSN: 09398368.
15. McGrath, B.P., Holmes, D.G., Lipo, T.A. (2001) *Optimized space vector switching sequences for multilevel inverters*, Proc. IEEE Applied Power Electronics Conf. (APEC), (2001), p. 1123–1129, DOI: 10.1109/APEC.2001.912507.
16. Krah, J., Holtz, J. (1999) *High performance current regulation and efficient PWM Implementation for low inductance servo motors*, IEEE Trans. Ind. Appl., Vol.36, No.5, (1999), p. 1039–1049, DOI: 10.1109/28.793364.
17. Somasekhar, V.T., Gopakumar, K. (2003) *Three-level inverter Configuration cascading two 2-level inverters*, IEE Proc. Electr. Power Appl., Vol.150, No.3, (2003), p. 245–254, DOI: 10.1049/ip-epa:20030259.
18. Kanchan, R.S., Baiju, M.R., Mohapatra, K.K., Ouseph, P.P., Gopakumar, K. (2005) *Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages*, IEE Proc.-Electr. Power Appl., Vol.152, No.2, (March 2005), p.297-309, DOI: 10.1049/ip-epa:20045047.
19. Baiju, M.R., Gopakumar, K., Mohapatra, K.K., Somasekhar, V.T., Umanand, L. (2003) *Five-Level inverter voltage-space vector phasor generation for an Open-End Winding Induction Motor Drive*, In: IEE proc.-power Appl.Vol.150, No.5, p.531-538, DOI: 10.1049/ip-epa:20030659.
20. G.Sambasiva Rao, K.Chandra Sekhar (2011) *A Twelve-Level Inverter System for Dual- Fed Induction Motor Drive*, International journal of advanced engineering sciences and technologies, Vol.6, No.2, (2011), p.157-167, ISSN: 2230-7818.

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