

IMPLEMENTATION OF PWM SOFT SINGLE SWITCHED DC-DC CONVERTERS WITH COUPLED INDUCTORS

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Abstract. This paper proposes a novel family of pulse width modulation of soft-single-switched dc-dc converters without high voltage and current stresses. These converters do not require any extra switch to achieve soft switching, which considerably simplifies the control circuit. In all converter family members, the switch is turned on under zero-current condition and is turned off at almost zero-voltage condition. From the proposed converter family, the boost topology is analyzed, and its operating modes are explained. The proposed circuit is simulated using MATLAB/Simulink.

Keywords: soft switching, zero voltage switching, zero current switching, PWM converters, MATLAB/Simulink

1. Introduction

Conventional hard switching converters possess increased size, weight, increased switching losses and electromagnetic interference. The switching devices used in DC converters with Pulse Width Modulation (PWM) control can be gated to synthesize desired shape of output voltage or output current at turn on and turn off conditions of switch. However the devices were turned on and off at a load current with high di/dt value. The switches were subjected to a high voltage stress and the switching power loss of device increases linearly with the switching frequency. The turn on and turn off loss could be a significant part of the total power loss. In order to solve the above issues soft switching converters are the need of the hour.

In recent years many research work were carried out in modernizing soft switching topologies in DC-DC converters. Soft switching converters are easy to control the output voltage to desired magnitude by Pulse Width Modulation (PWM) technique. Among the converter topologies quasi resonant converter topologies does not have extra switches to obtain soft switching conditions. They have major drawback of variation of the switching frequency [1]. The complexity of power and control circuit was increasing under zero voltage transition and zero

Current transition constituting PWM based control by usage of two switches to achieve soft switching [3-10]. The analysis and experimental results of a buck quadratic PWM soft switching converter and improved Boost PWM soft single switched converter with single switch were presented in [10-12] but voltage stresses and current stresses is more vulnerable in switches. PWM based

SSS converters provide a solution to the problems faced by converter topologies [11-13]. An improved version of boost PWM SSS converter with low voltage and current stresses have been adopted to overcome above drawbacks but usage of large number of passive components make the converter implementation difficult [14]. The operation and properties of ZCT-PWM were compared with other converter topologies and discussed in [15]. A systematic approach to developing soft switching PWM converters based on synchronous switch is presented in [16]. A novel method is applied to isolated converters topologies this method provide soft switching condition for all the switching elements [18]. A novel family of pulse width modulation soft single switched DC-DC converter without high voltage and current stresses is been described.

2. Soft switching

The switching techniques in the resonant converter employ zero voltage switching and/or zero current switching. In zero current switching, the device turns-on with zero current and turns off after the current drops to zero. In zero voltage switching, the switch turns-off at zero voltage and turns-on after the device voltage drops to zero. Figure 1 illustrates the ZVS and ZCS switching trajectory. In the ZVS converters, the voltage across the device is brought to zero by external means, just prior to turn-on, thus eliminating the turn-on losses.

During the turn-off process, the rate of voltage raise is limited by external means (by a capacitor in shunt with the main switch), so that the device current falls to zero before the voltage raises substantially i.e. assisted turn-off.

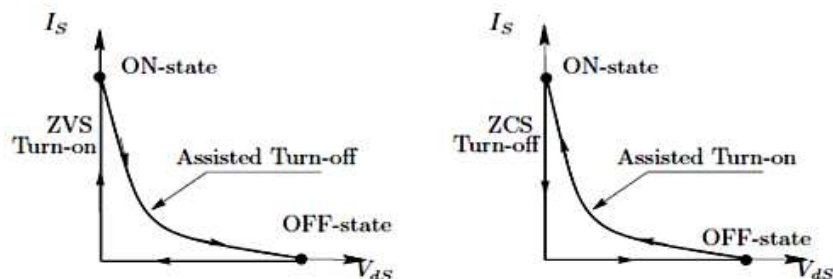


Figure1. Switching strategy

In the ZCS converters, the current through the device is brought to zero by external means, just prior to turn-off. Thus the turn-off losses as well as the voltage spikes due to stray inductance are totally eliminated. During the turn-on process, the current raise is slowed down by external means (by an inductor in series with the main switch), so that the device voltage falls to zero before the current becomes appreciable i.e. assisted turn-on.

A resonant switch is a sub-circuit comprising a semiconductor switch S and resonant elements, L_r and C_r . The switch S can be implemented by a unidirectional or bidirectional switch, which determines the operation mode of the resonant switch. Two types of resonant switches, including zero-current (ZC) resonant switch and zero-voltage (ZV) resonant switches, are shown in Figure 2 and Figure 3, respectively.

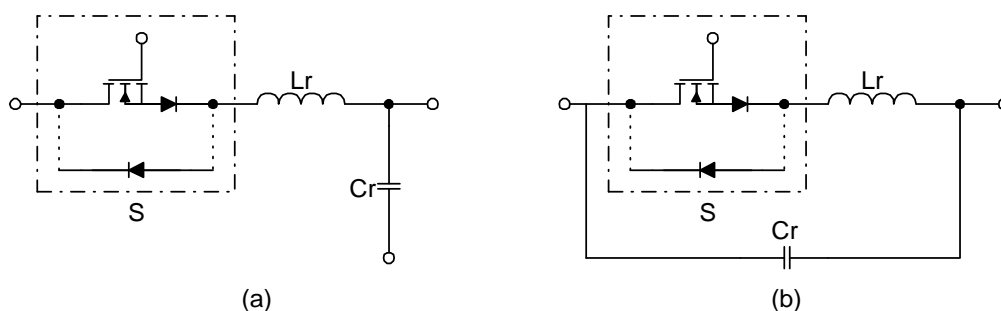


Figure 2. Zero-current (ZC) resonant switch

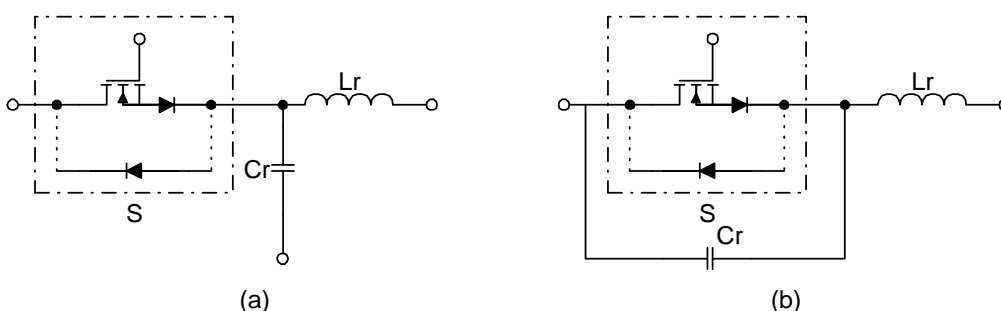


Figure 3. Zero-voltage (ZV) resonant switch

3. Soft switching PWM converters

The soft switching PWM converter is defined here as the combination of converter topologies and switching strategies that result in zero-voltage and/or zero-current switching. They are called also pseudo-resonant, quasi-resonant, resonant transition, clamped voltage topologies and other. In these converters the resonant transition is employed only during a short switching interval. The output voltage is usually controlled by PWM with constant switching frequency.

Soft switching PWM converters can be classified as follows:

1. ZVS PWM converters
2. ZCS PWM converters
3. ZVS ZCS PWM converters

3.1. ZVS PWM converters

The simplest ZVS PWM full bridge converter is shown in Figure 4. The converter snubbers consist of capacitances C_1-C_4 and inductance L_R , which are represented by transistor and diode output

capacitances and transformer leakage inductance respectively.

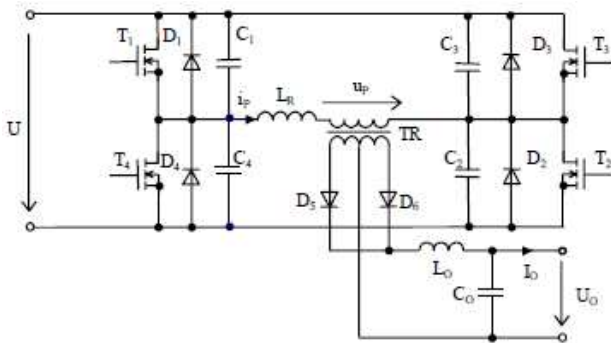


Figure 4. Full-Bridge ZVS PWM converter

The transistors (MOSFETs or IGBTs) in leading or lagging leg are turned-on while their respective anti-parallel diodes conduct. Since the transistor voltage is zero during the entire turn-on transition, switching loss does not occur at turn-on.

By utilizing small snubber capacitors C_1 – C_4 the turn-off losses are sufficiently reduced. If the transistor turn-off time is sufficiently fast, then the transistor is switched fully off before the collector voltage rises significantly above zero, and thus negligible turn-off switching loss is incurred. The ZVS converter exhibits low primary-side switching loss and generated EMI. However, conduction losses are increased with respect to an ideal hard switching PWM full bridge topology. Figure 5 and Figure 6 show voltage current relationship during ZVS process.

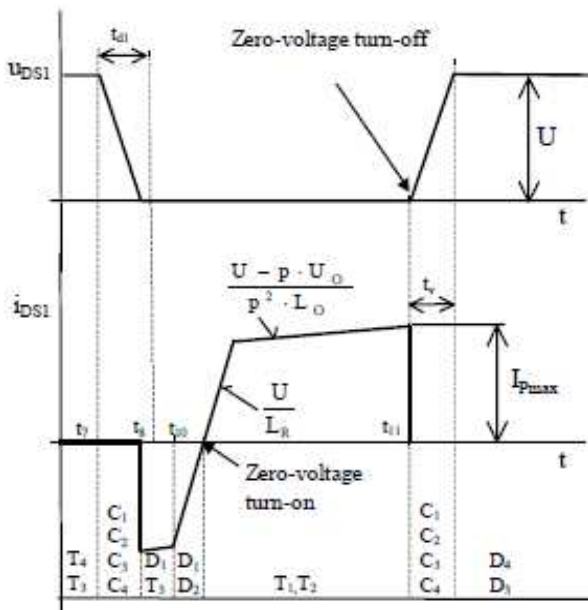


Figure 5. Switch (transistor MOSFET T_1 and its body diode D_1) voltage U_{ds1} and current I_{ds1} during turn-on and turn-off (leading leg)

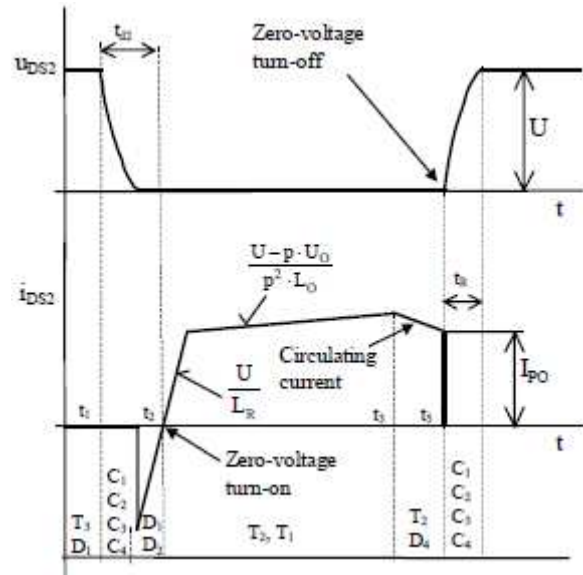


Figure 6. Switch (transistor MOSFET T_2 and its body diode D_2) voltage U_{ds2} and current I_2 during turn-on and turn-off (lagging leg)

At light load, the leakage inductance energy is not sufficient to ensure zero-voltage switching in the lagging leg of the converter. This critical load condition is also a function of the line condition. The worst case is high input voltage when more capacitive energy is required. Another consideration is the delay time from the turn-off T_4 until the turn-on of T_1 and vice versa. If the delay time t_d is too short, then the device capacitance may not be fully discharged. However, if the delay time t_{d2} is too long, the capacitor voltage will peak, continue to resonate and drop. Fortunately, the time of peak charge is relative independent of the input voltage and load condition and is equal to one quarter of $L_r C$ time constant.

The secondary-side diodes switch at zero current. This leads to switching losses and ringing as a result of interaction of diodes capacitance with the leakage inductance of the transformer. Additional snubber circuitry is usually required, for prevention of excessive diode voltage stress. To remove the above-mentioned disadvantages a lot of derivations of the ZVS PWM converters were developed. The penalty for the improvement is usually higher complexity of the converter topology.

3.2. ZCS PWM converters

The ZCS PWM converters can be derived from the ZVS PWM converters by applying the duality principle. The transformer leakage inductance, the rectifier's junction capacitances, and the transformer winding capacitances can be utilized in

this circuit. Similar to the FB-ZVS-PWM converter, the FB-ZCS-PWM converter also uses phase-shift control at constant switching frequency to achieve required converter operation. The switches must have reverse-voltage blocking capability. The switch can be implemented by an IGBT or a MOSFET in series with a reverse blocking diode, an IGBT with reverse-voltage blocking capability, a MCT, or a GTO. An important advantage of the circuit is that the rectifier diodes do not suffer from reverse recovery problem since they commute with zero-voltage switching. Figure 7 shows Full bridge ZCS Pulse width Modulation Circuit whereas Figure 8, Figure 9 and Figure 10 show the corresponding turn-on turn-off operations.

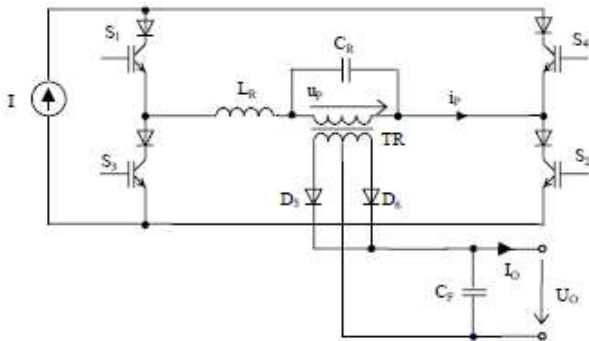


Figure 7. Basic circuit diagram of the FB-ZCS-PWM converter

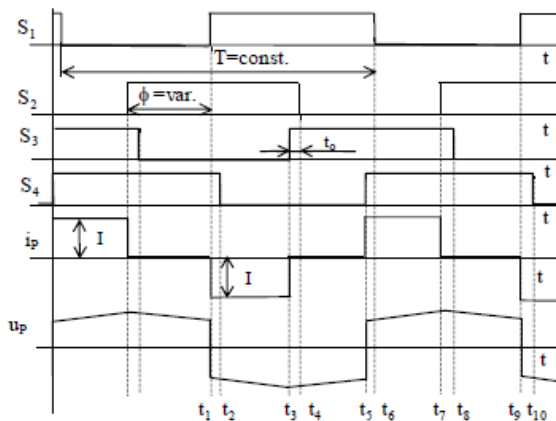


Figure 8. Idealized waveforms of the FB-ZCS-PWM converter

This feature makes the converter attractive for applications with high output voltage e.g. power factor correction circuits, where the rectifiers suffer from severe reverse-recovery problems when conventional PWM, ZVS-QRC, or ZVS-PWM converter techniques are used. The efficiency of the converter drops significantly at low line and heavy load since the switches begin to lose zero current switching.

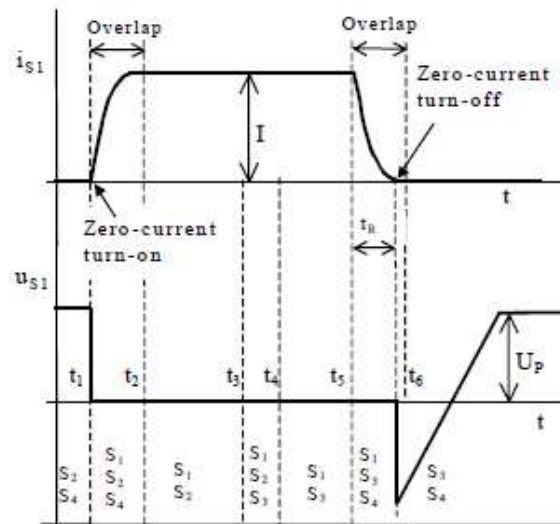


Figure 9. Switch S1 voltage and current during turn-on and turn-off

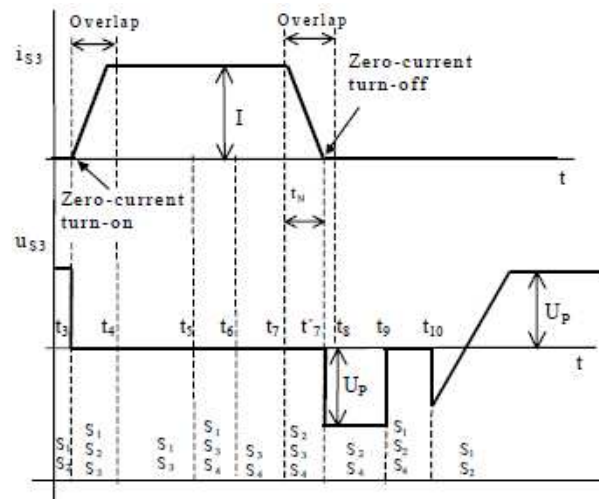


Figure 10. Switch S3 voltage and current during turn-on and turn-off

The Table 1 shows comparison of various parameters for two configurations FB-ZVS-PWM and FB-ZCS-PWM.

Table 1. Some dual characteristics of the FB-ZVS-PWM converter and FB-ZCS-PWM converter

	FB-ZVS-PWM	FB-ZCS-PWM
Topology type	Buck type	Boost Type
Switching conditions for active switches	Zero voltage switching	Zero current switching
Switching conditions for rectifiers	Zero current switching	Zero voltage switching
Soft switching easy to achieve at	Heavy load	Light Load
Implementation of active switches	Diode in parallel with transistor	Diode in series with transistor

3.3. Zero-voltage zero-current switching PWM converters

The operating frequency of IGBTs is normally limited to 20-30 kHz because of their current tailing problem. To operate IGBTs at higher switching frequencies, it is required to reduce the turn-off switching losses. ZVS with substantial external capacitor or ZCS can be a solution. The ZCS, however, is deemed more effective since the minority carriers are swept out before turning off.

The zero-voltage zero-current switching (ZVZCS) PWM converters are derived from the full-bridge phase-shifted zero-voltage (FB-PS-ZVS) PWM converters. The PS-ZVS-PWM converter is often used in many applications because this topology permits all switching devices to operate under zero-voltage switching by using circuit parasitic such a transformer leakage inductance and devices junction capacitance.

However, because of phase-shifted PWM control, the converter has a disadvantage that circulating current flows through a transformer and switching devices during freewheeling intervals.

The circulating current is a sum of the reflected output current and transformer primary magnetizing current. Due to circulating current, RMS current stresses of the transformer and switching devices are still high compared with that of the conventional hard-switching PWM full-bridge converter. To decrease the circulating current to zero and thus to achieve zero-current switching for lagging leg, various snubbers and/or clamps connected mostly at secondary side of transformer are applied.

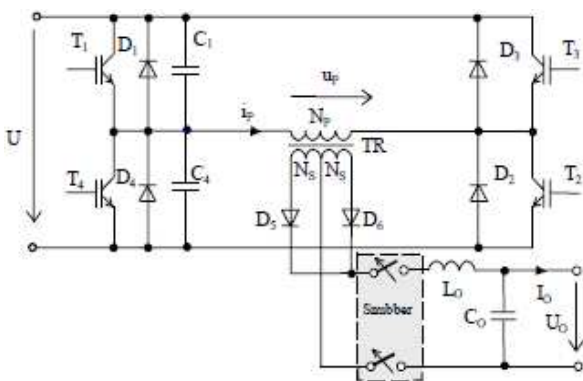


Figure 11. Principle of the ZVZCS converter operation

Hence, the converter achieves nearly zero-current switching for the lagging leg (transistors T_2 , T_3) due to minimized circulating current during interval of lagging leg transition and achieves zero-voltage switching for leading leg (transistors T_1 and T_3). An example of ZVZCS PWM converter is

shown in Figure 12. ZVS of the leading leg is achieved by the same manner as that of the ZVS full-bridge PWM converter, while the ZCS of the lagging leg is achieved by resetting the primary current during freewheeling period by using active clamp in the secondary side, which needs an additional active switch. Oscillogram of the collector-emitter voltage V_{CE2} and collector current I_{CE2} in the lagging leg at turn-on and turn-off. The transistor is turned-on at zero voltage and turned-off at zero current. The circulating current does not occur, only negligible magnetizing current flows during freewheeling interval through primary winding of transformer. This combination of switching is very effective for IGBT transistors, which have problems at turn-off due to tail current effect. The converter is operating very well at nominal load, but it is not capable operating over wide load range (from no-load conditions to short circuit) with zero-voltage or zero-current switching for all power switches.

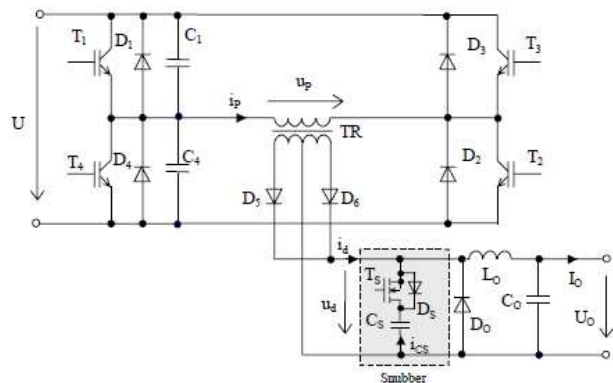


Figure 12. ZVZCS DC-DC PWM converter

The auxiliary transformer TR_2 is the main part of the auxiliary circuits in this converter. The transformer TR_2 should have considerably large air-gap to ensure sufficiently high magnetizing current I_{m2} and at the same time to prevent core saturation. The saw-tooth magnetizing current I_{m2} ensures the zero-voltage turn-off of the transistors T_1 , T_4 not only at light load but also at no-load conditions. Simultaneously, charging or discharging of the capacitors C_1 , C_4 by magnetizing current i_{m2} avoids high current spikes at transistors T_1 , T_4 turn-on at light load and no-load.

In order not to lose the zero-current turn-off of the transistors T_2 , T_3 at short circuit, it is necessary to charge up the capacitor C_s to the rated value of the voltage. The capacitor C_s can be charged from the rectifier GB_1 , which is connected to the secondary winding of the auxiliary transformer TR_2 .

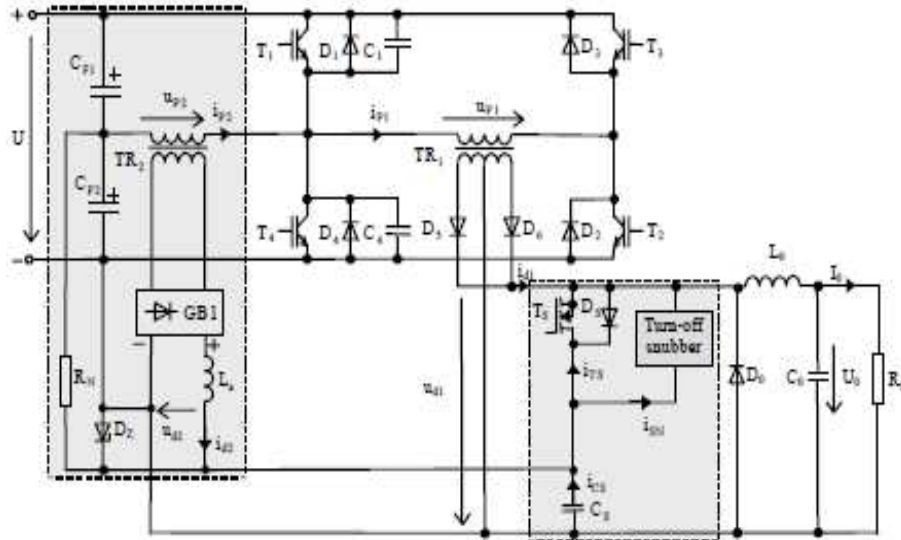


Figure 13. Improved ZVZCS DC-DC PWM converter

Soft switching and reduction of circulating currents for full load range are achieved in this converter. The converter is especially suited for application where short circuit and no-load are normal states of the converter operation, e.g. arc welding. Figure 11 and Figure 13 shows the two versions of combination of ZVS and ZCS configurations.

4. Simulation results

4.1. Proposed circuit diagram

The PWM controlled soft single switched boost converter circuit diagram as shown in the Figure 14. It is used for less DC voltages to high DC voltages with minimum switching loss and less voltage stress.

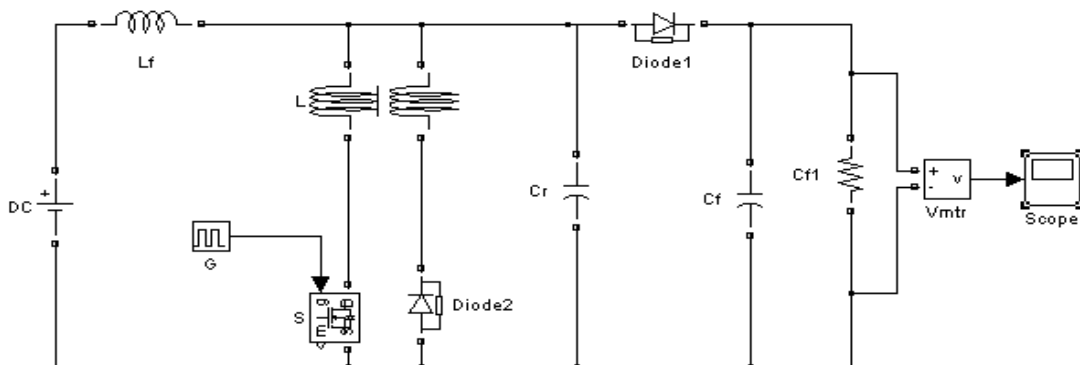


Figure 14. Proposed circuit diagram

Figure 16 shows the input voltage and Figure 17 shows the gate pulse and V_{ds} voltage across switch whereas figure 18 shows output current.

Figure 15 shows the output voltage and Figure 19 shows the comparison graph between input (v_s) output voltage.

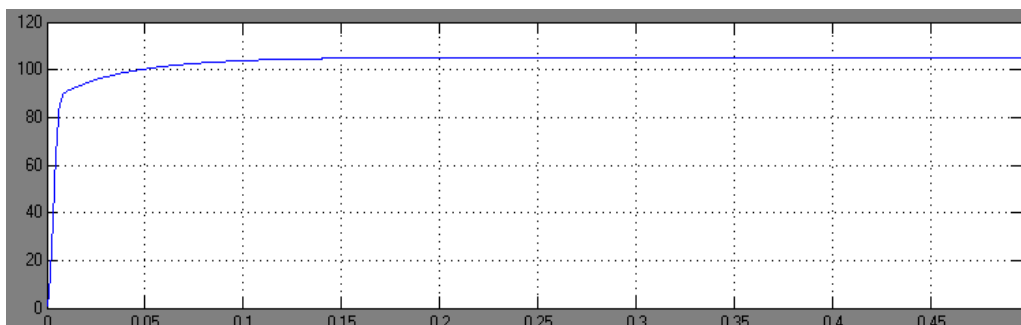


Figure 15. Output voltage

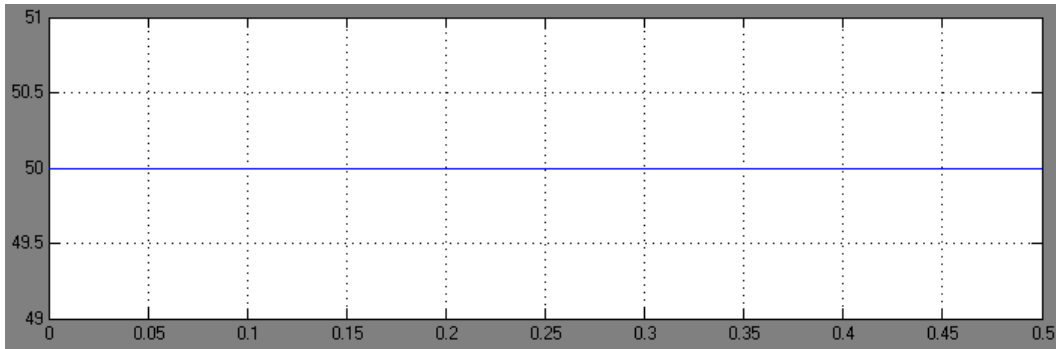


Figure 16. Input DC voltage

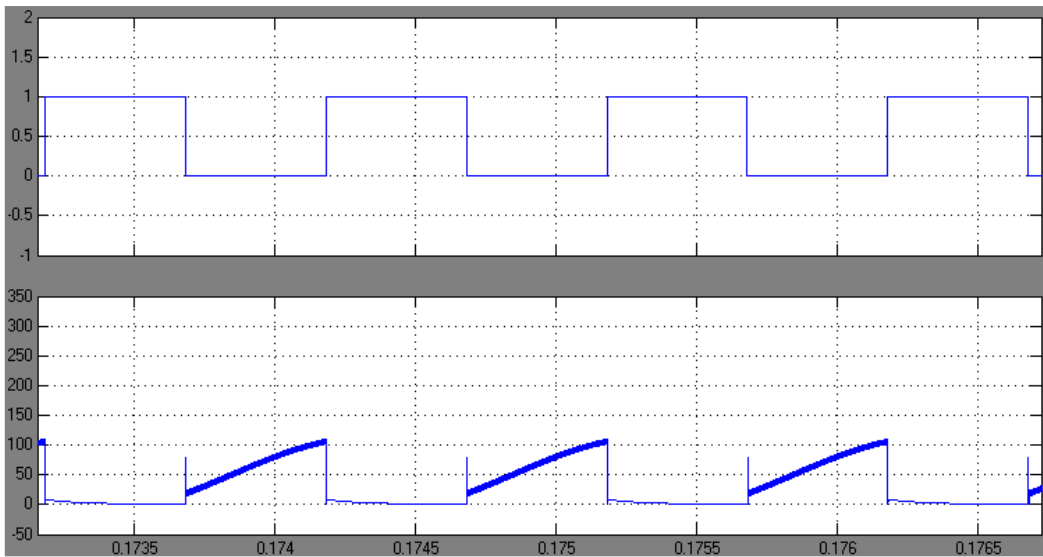


Figure 17. Switching pulse (ii) corresponding voltage across the switch

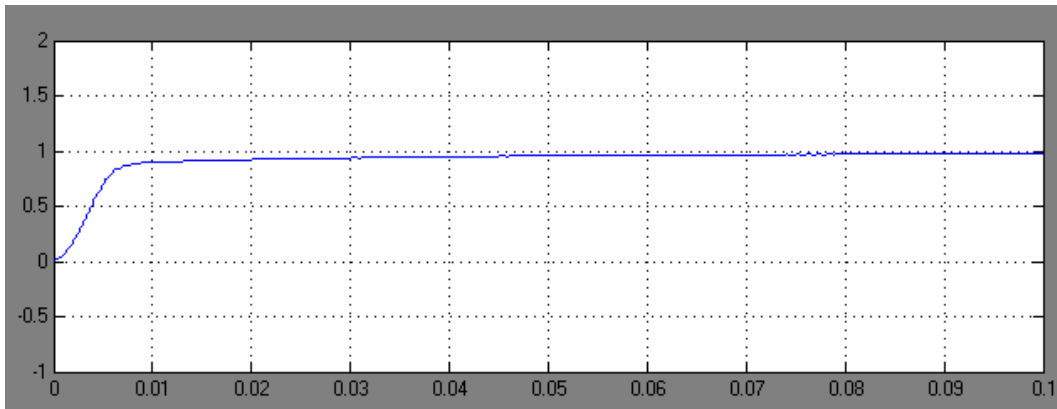


Figure 18. Output current

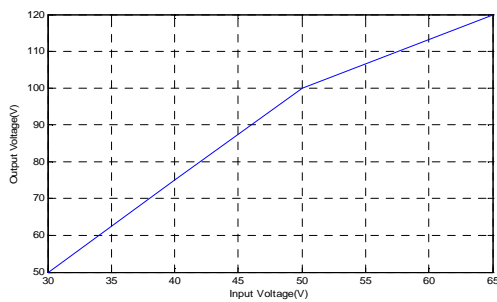


Figure 19. Comparison of input vs. output voltage

4.2. Voltage stress

Figures 20 and 22 shows the conventional and proposed boost circuit diagrams. Figures 21 and 23 shows the gate pulse and switch voltage for conventional and proposed circuit diagram. From Figure 21 conventional circuit has high voltage stress and no ZVS switching. From Figures 21 and 23 it is seen that proposed circuit reduces the voltage stress.

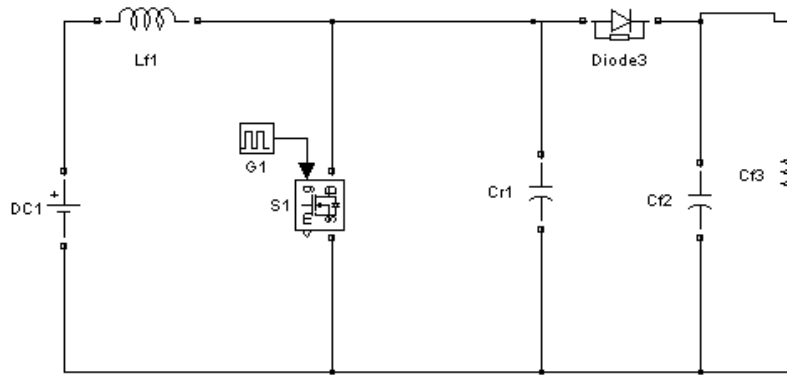


Figure 20. Conventional boost converter

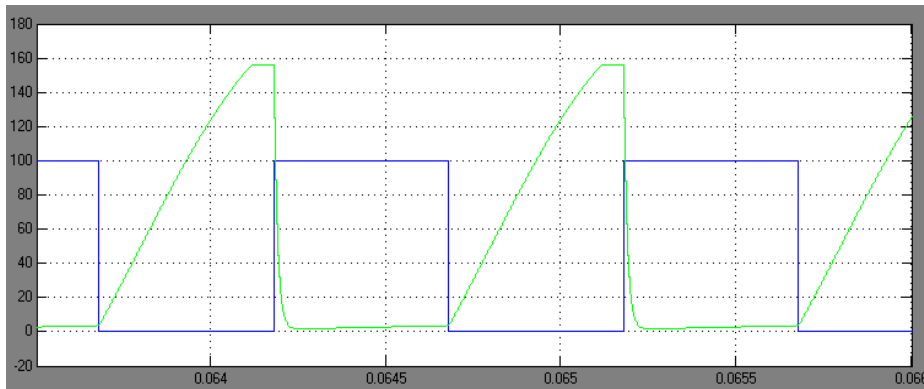


Figure 21. Gate pulse and V_{ds} voltage

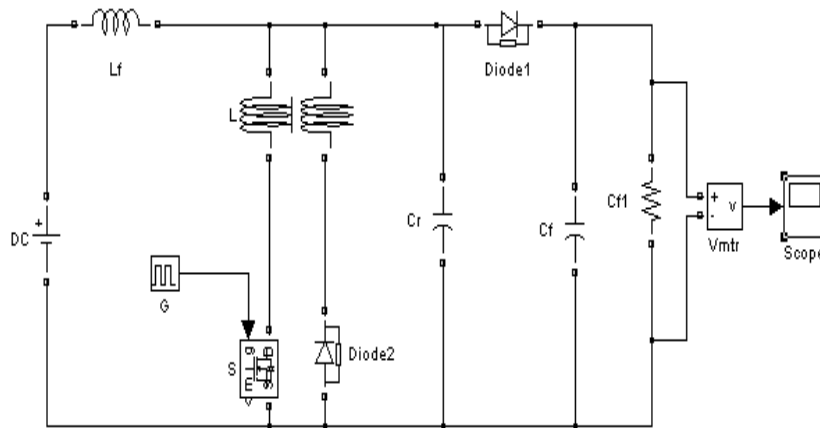


Figure 22. Proposed circuit diagram

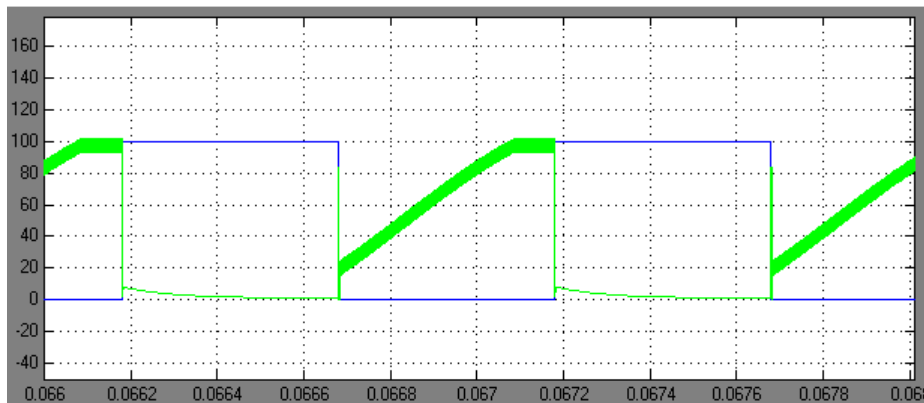


Figure 23. Gate pulse and V_{ds} voltage

4.3. Open loop system

Figure 24 shows the open loop system circuit diagram. In this circuit initially 50Volts is applied

after 0.4 sec 10% voltage should be raised. The output voltage changes with respect to input voltage. It is shown in Figures 25 and 26.

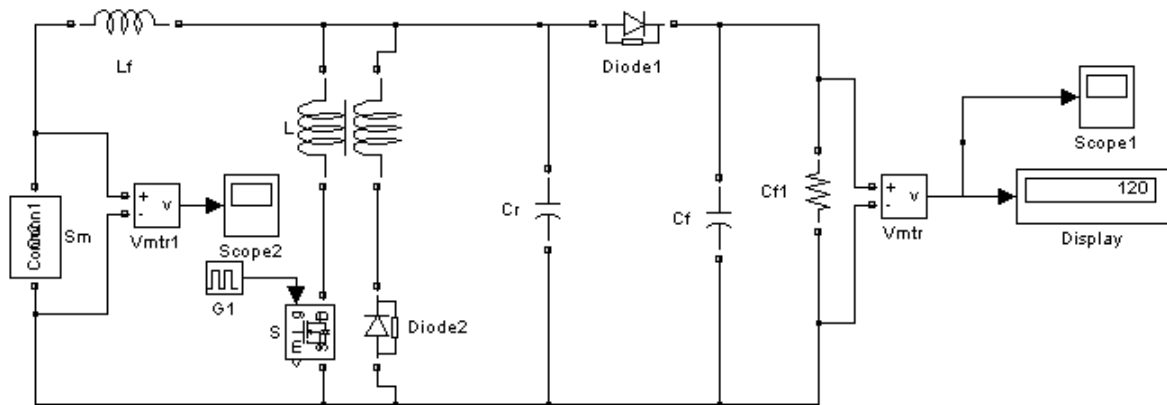


Figure 24. Open loop circuit diagram

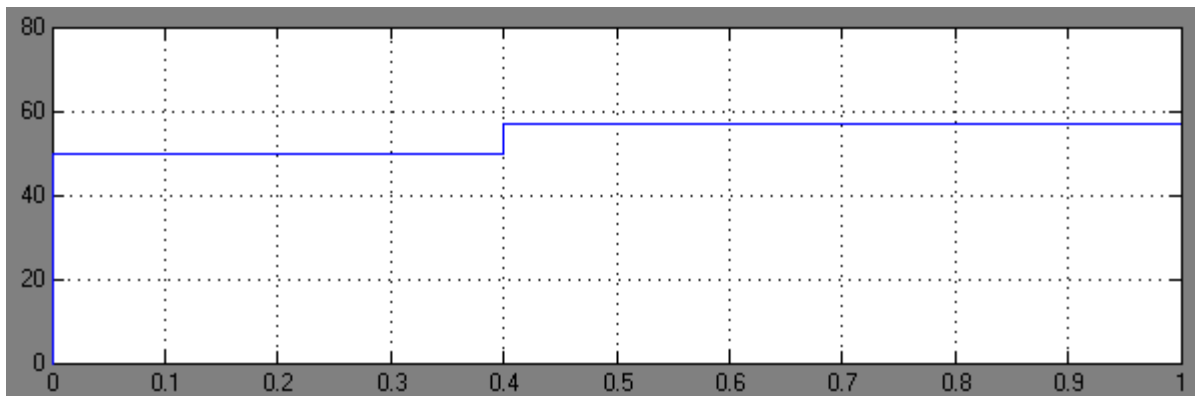


Figure 25. Input voltage with disturbance

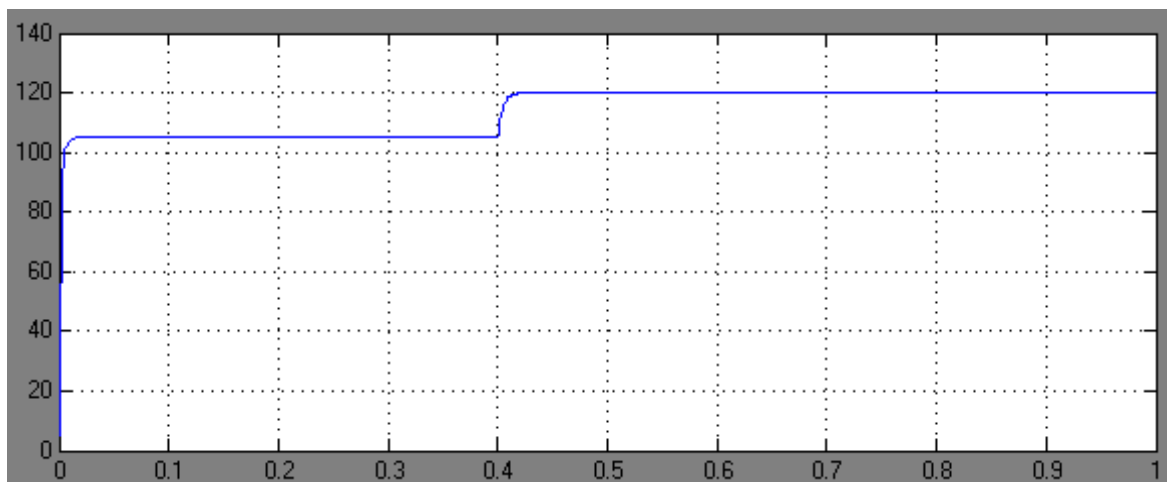


Figure 26. Output voltage with disturbance

4.4. Closed loop system

Closed loop system is used to control the output voltage. The output voltage is compared with set value. Comparator gives the difference between two signals it is called as error. Error signal is given to PI controller. PI controller adjust K_p and

K_i gains based on the error signals. It is compared with one triangle carrier signal. It generates a PWM pulse. It is given to MOSFET thus PWM pulse is generated. It is control the output voltage. Figure 27 shows the closed loop system and Figure 28 shows the regulated output voltage with disturbance.

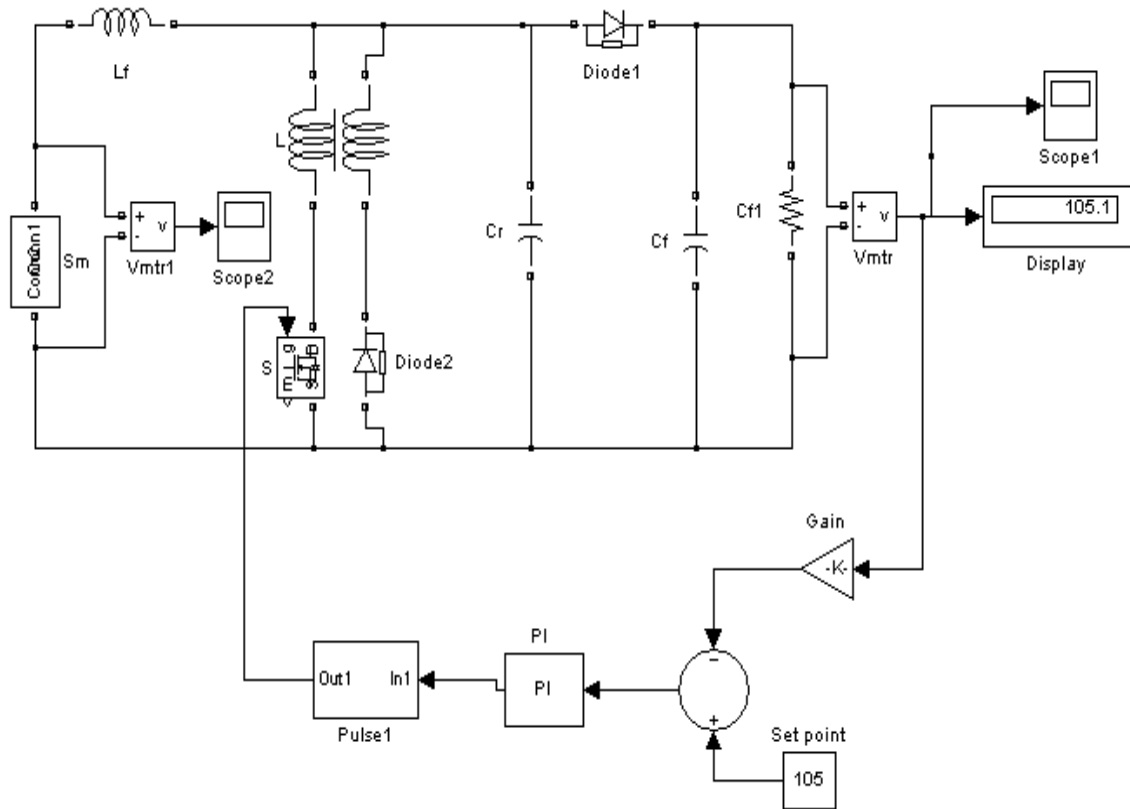


Figure 27. Closed loop circuit diagram

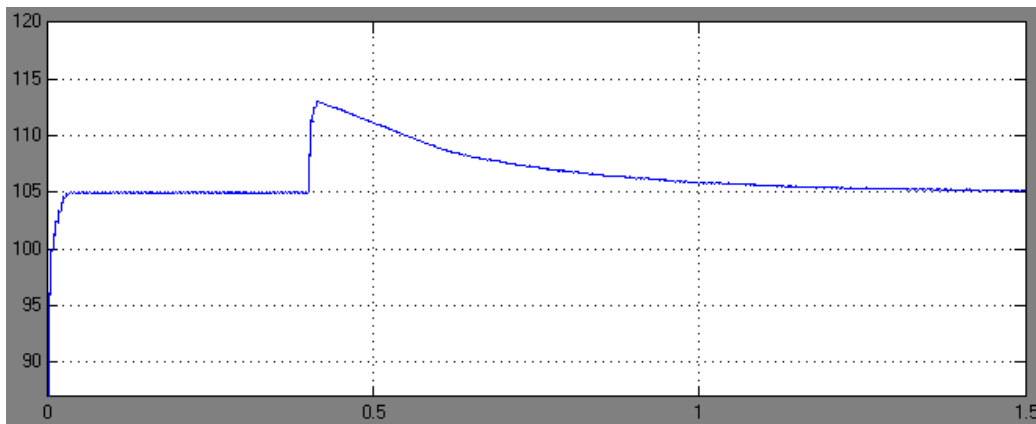


Figure 28. Output voltage with disturbance

From the Table 2 it is inferred that our proposed boost converter reduces the percentage of voltage regulation compared to conventional closed loop boost converter.

Table 2. The comparison of conventional and proposed closed loop boost converters

Converter type	Output voltage	Voltage regulation
Conventional closed loop converter	114.5	9.5%
Proposed closed loop converter	105.1	0.1%

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Received in January 2014
(and revised form in February 2014)