Simulation of Three-Level Diode Clamped Multilevel Inverter Using SPWM Technique, Space Vector Strategy & SHE Technique

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Abstract
The multilevel began with the three level converters. The fundamental thought of a multilevel converter to fulfill higher power to use a progression of power semiconductor switches with a few lower voltage dc source to perform the power transformation by combining a staircase voltage waveform. Regardless, the output voltage is smoother with a three level converter, in which the output voltage has three conceivable values. This results in less harmonics, yet on the other hand it has more sections and is more unpredictable to control. In this project, three level inverter topologies and Sinusoidal pulse width modulation, Selective harmonic elimination and Space vector strategy has been connected to characterize the exchanging example for three level inverter that minimize the harmonic distortion at the inverter output. Mat lab Simulation result will be analyzed.

Keywords
SPWM (sinusoidal pulse width modulation), THD (total harmonic distortion), Space vector, SHE (selective harmonic elimination)

1. Introduction

Now a day's several industrial applications have begun to need high power. Some appliances within the industries but need medium or low power their operation. Using a high power supply for all industrial loads might prove helpful to some motors requiring high power, whereas it should harm the other loads. Some medium voltage motor drives and utility applications need medium voltage. In this project we have a tendency to done three different types of modulation techniques and conclude the THD for all the modulation techniques. From this we will understand that within which modulation technique the most quantity of input voltage issued by knowing the THD [1].

Types of Multilevel Inverters

Multilevel inverters are three types:

1) Diode clamped multilevel inverter;
2) Flying capacitors multilevel inverter;
3) Cascaded H-bridge multilevel inverter.

2. Diode Clamped Multilevel Inverter

The main idea of this inverter is to use diodes and provides the multiple voltage levels through the various phases to the electrical device banks that are in series [2]. A diode transfers a restricted quantity of voltage, thereby reducing the strain on different electrical devices. The most output voltage is half the input DC voltage. It's the most downside of the diode clamped structure electrical converter. This drawback may be resolved by increasing the switches, diodes, capacitors. Attributable to the capacitor equalization problems, these are restricted to the three-levels. This kind of inverters provides the high efficiency as a result of the fundamental frequency used for all the change devices and it's a simple technique of the rear to back power transfer systems.

An m level inverter leg requires 2·(m– 1) switching devices and (m– 1)·(m– 2) clamping diodes. For a three-level inverter, m = 3, so it needs four switching devices and two clamping diodes per leg as shown in Figure 1.

1. For an output voltage of $V_a = V_{dc}$, all the upper-half switches of a-phase leg are turned ON, i.e., S1 and S2 are ON.
2. For output voltage of $V_a = V_{dc}/2$, only S2 and S3 are ON
3. For output voltage of $V_a = 0$, all the lower-half switches of a- phase leg are turned ON, i.e., S3 and S4 are ON.

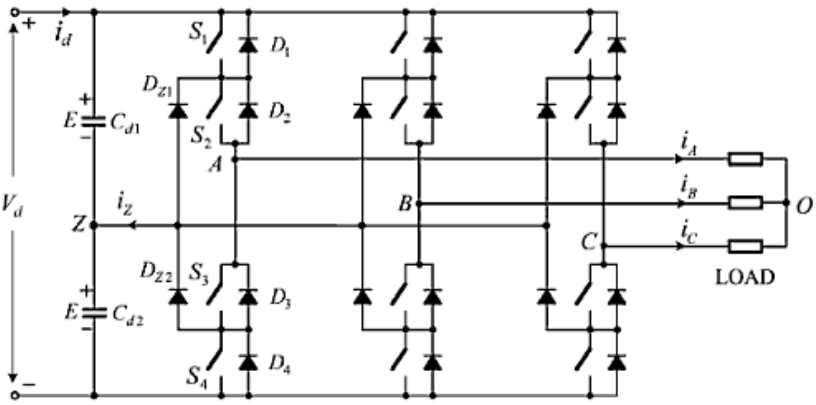

Fig. 1. Three-level diode clamped inverter

Table1 shows the voltage levels and their corresponding switch states. State condition "1"means the switch is ON, and state "0" suggests that the switch is OFF. It should be noticed that there are two complementary switch pairs. These pairs for one leg of the inverter are (S1, S3) and (S2, S4).

Table 1. Switch states for various voltages of a phase leg

Voltage level V_a=	S_{A1}	S_{A2}	S_{A3}	S_{A4}
V_{dc}	1	1	0	0
$V_{dc}/2$	0	1	1	0
zero	0	0	1	1

Thus, if one among the complementary switch pairs is turned ON, the other often same try should be OFF. Two switches area unit always turned ON at the same time. Output voltage waveform of a three-level inverter is as shown in Figure 2.

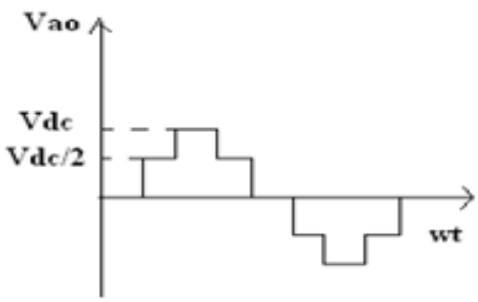

Fig. 2. Output voltage waveform of a three level inverter

PWM Techniques

1. Sinusoidal Pulse Width Modulation (SPWM)
2. Space Vector Modulation (SVM or SVPWM)
3. Selective Harmonic Elimination (SHE)

3. Sinusoidal Pulse-Width Modulation

In this theme, three sinusoidal reference waves every shifted by 120°areused, Figures 3, 4 and 5. A triangular carrier wave is compared with the reference signal similar to a phase to generate the gating signals for that phase [3]. Magnitude and frequency of resultant wave depends on the magnitude and frequency of carrier wave. Within the gift configuration, modulation index (which could be a quantitative relation of peak price of reference wave to peak price of carrier wave) is varied within the vary 0.7-0.95. In multiple-pulse modulation, all pulses are an equivalent width. Vary the pulse width in step with the amplitude of a sine wave evaluated at the middle of an equivalent pulse.

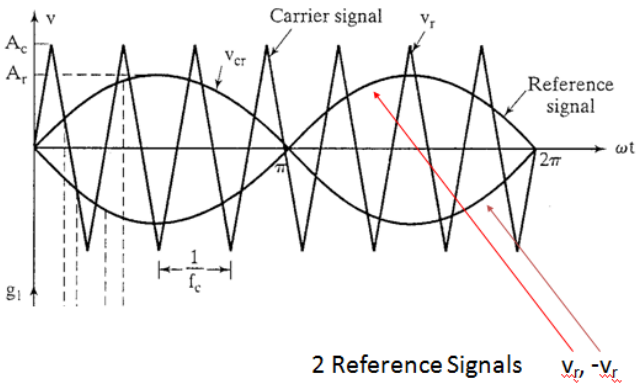

Fig. 3. Generate the gating signal

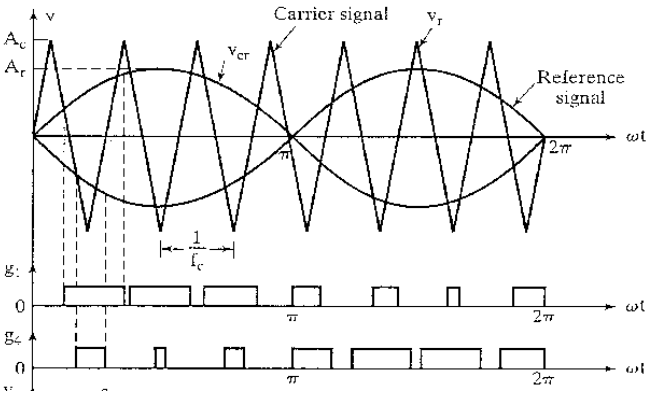

Fig.4. Comparing the carrier and reference signals

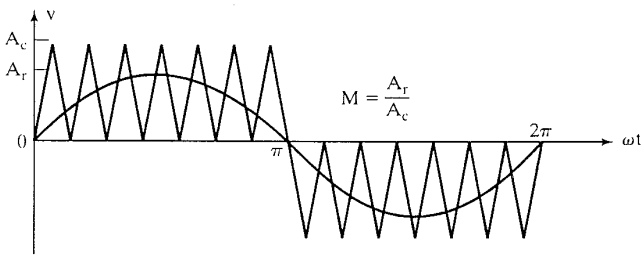

Fig.5. Generate the same gate pulses with one sine wave

Variation of THD with modulation index in sinusoidal PWM method

Modulation index can be defined as

m = Peak value of Sin wave/peak value of Triangular wave

4. Space Vector Modulation

Space vector pulse width modulation (SVM) is kind of totally different from the PWM strategies. With PWM the inverter is thought of as three separate push-pull driver stages that produce every

phase waveform severally. SVM but treats the inverter as a single unit. Specifically the inverter is driven to eight distinctive states. Modulation is accomplished by change the state of inverter[4]. SVM could be a digital modulation technique wherever the target is to come up with PWM water line voltages. This is often wiped out every sampling period by properly choosing the change states of inverter.

Stationary Space Vectors

Three switching states ([1], [0] and [- 1]) will represent the operation of each leg. By taking all three phases into account, the inverter includes a total of 27 possible switching states [5]. The chance of three

section switching states that area unit pictured by three letters in square brackets for the inverter phases A, B, and C. The voltage has four groups.

(a) Zero vector (V_1, V_2, V_3), representing three switching states [1 1 1], [-1 -1 -1] and [0 0 0]. The magnitude of V_1, V_2, and V_3 is zero.

(b) Small vector (V_4 to V_{15}), all having a magnitude of $V_d/3$. Each small sector has two switching states, one containing [1] and the other containing [-1] and they classified into P- or N-type small vector.

(c) Medium vectors (V_{17}, V_{19}, V_{21}, V_{23}, V_{15}, V_{27}), whose magnitude is ($\sqrt{3}/3$) V_d.

(d) Large vectors (V_{16}, V_{18}, V_{20}, V_{22},V_{24}, V_{26}), all having a magnitude (2/3) V_d.

The Switching States by Using Switching Sequence

By considering the switching transition and using sequences direction, shown in Figures 6 and 7, the direction of the switching sequences for all regions in six sectors is derived and the switching orders are noted, that are obtained for every region situated in sectors I to VI, if all switching states in every region are used simulation and implementation of three-level inverter to boost the facility quality. The three-level inverter is additionally capable of improving AC power. It's the most important power electronic system for reducing harmonics distortion in associate electrical power system.

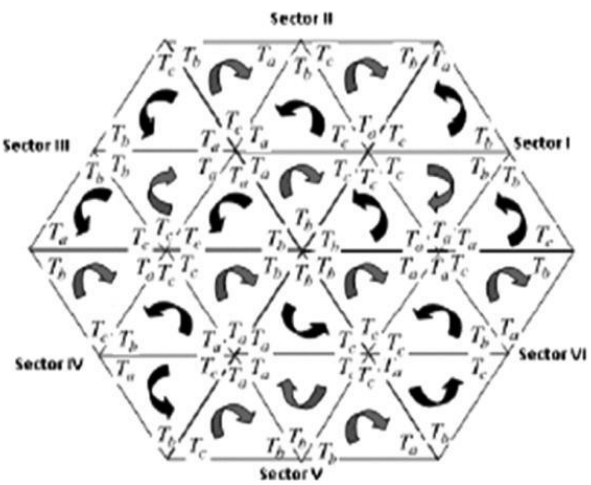

Fig. 6. Switching sequence for three-level SVPWM

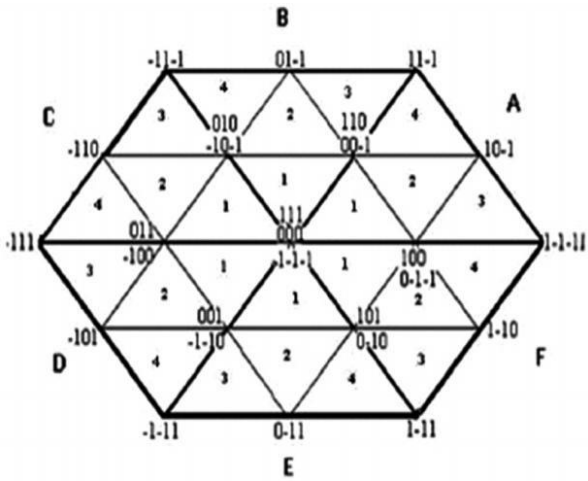

Fig. 7. Sectors and their regions for three-level inverter

5. Selective Harmonic Elimination

Two major approaches are projected to eliminate low frequency harmonics:

1) Increasing the switching frequency in sinusoidal-triangular Pulse width Modulation (PWM) and space vector PWM for two-level inverters or adopting phase shift in multicarrier based PWM for multi level inverters.
2) Optimizing switch angles for selected harmonics elimination (SHE). For medium and high voltage/power applications, the primary approach and also the variety of switch angles are restricted by switch loss, and typically are used once the available voltage steps are restricted.

Selected harmonics elimination based methods have been proposed for both two-level and multilevel inverters. This section is focusing on the SHE based methods for multilevel inverters. Ideally, in the multilevel inverters, for every voltage level, there could be multiple switching angles. The number of eliminated harmonics is decided by the number of voltage steps and number of switching angles in each voltage step. However, because of the complexity of the problem, most studies proposed so far are for one switching angle per one voltage level, as shown in Figure 8. This also means that the switching frequency in these methods can be as low as the fundamental frequency.

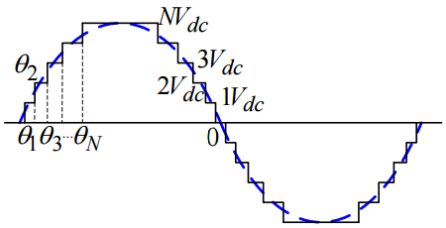

Fig. 8. Staircase waveform in multilevel inverters

In this case, the Fourier series expansion of the staircase waveform can be expressed as

$$V(\omega t) = \sum_{m=1,3,5,\ldots}^{\infty} \frac{4V_{dc}}{m\pi}(\cos(m\theta_1) - \cdots + \cos(m\theta_N))\sin(m\omega t) \tag{1}$$

Where N is the number of switching angels and m is the harmonic order.

Based on above equation, the following polynomial equation group can be formed to calculate the switching angles in order to realize the selected harmonics elimination for the multilevel inverter:

$$\begin{cases} \frac{4V_{dc}}{\pi}(\cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) - \cos(\theta_4) + \cos(\theta_5) - \cdots + \cos(\theta_N)) = V_F \\ \cos(5\theta_1) - \cos(5\theta_2) + \cos(5\theta_3) - \cos(5\theta_4) + \cos(5\theta_5) - \cdots + \cos(5\theta_N) = 0 \\ \cos(7\theta_1) - \cos(7\theta_2) + \cos(7\theta_3) - \cos(7\theta_4) + \cos(7\theta_5) - \cdots + \cos(7\theta_N) = 0 \\ \cos(11\theta_1) - \cos(11\theta_2) + \cos(11\theta_3) - \cos(11\theta_4) + \cos(11\theta_5) - \cdots + \cos(11\theta_N) = 0 \\ \ldots \\ \cos(m\theta_1) - \cos(m\theta_2) + \cos(m\theta_3) - \cos(m\theta_4) + \cos(m\theta_5) - \cdots + \cos(m\theta_N) = 0 \end{cases} \tag{2}$$

In this equation group, the primary equation guarantees the specified elementary element, VF. The opposite equations are used to confirm the elimination of fifth, 7th, 11th..., and mth harmonics. It's clear that with N change angles, N-1 selected harmonics may be eliminated. The SHE waves planned in basically square measure ways attempt to solve the higher than equation cluster with totally different approaches. However, as a result of the character of high order polynomial equation groups, there are many disadvantages of those types of ways.

6. Results

SPWM:

Figure 9 shows the MATLAB simulation of three-level diode clamped inverter of SPWM Technique and the output voltage waveforms of SPWM are shown in Figure 10. Additionally by the FFT analysis we got the THD of 57.87% of SPWM Technique is shown in Figure 11.

SVM or SVPWM:

Figure 12 shows the MATLAB simulation of three-level diode clamped inverter of SVM Technique and the output voltage waveforms of SVM are shown in Figure 13. Moreover by the FFT analysis we got the THD of 32.83% of SPWM Technique is shown in Figure 14.

SHE:

Figure 15 shows the MATLAB simulation of three level diode clamped inverter of SHE Technique and the output voltage waveforms of SHE are shown in Figure 16. Also by the FFT analysis we got the THD of 41.22% of SPWM Technique is shown in Figure 17.

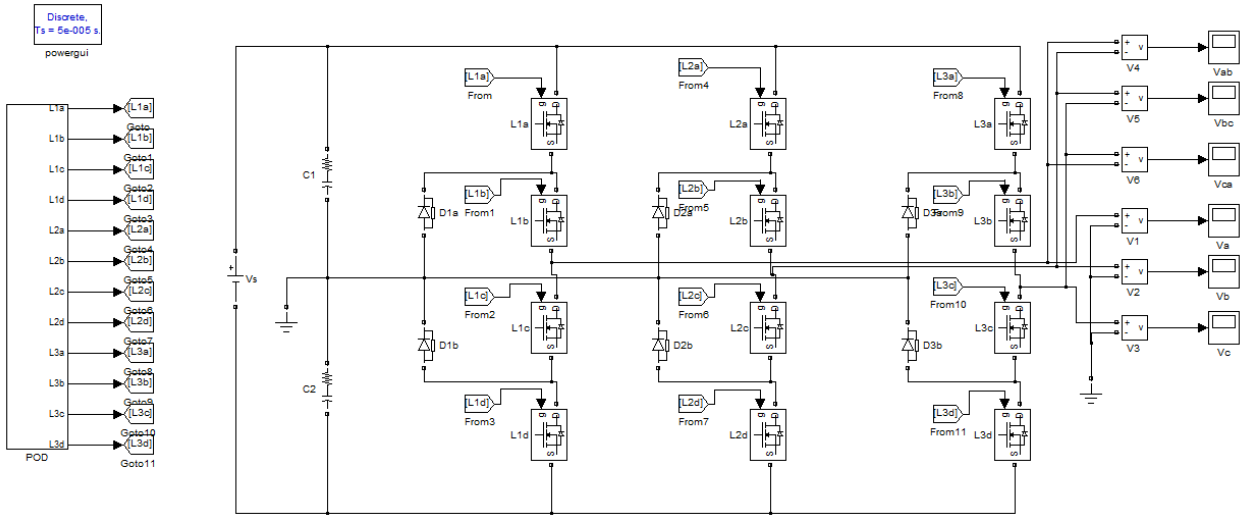

Fig. 9. SPWM circuit in MATLAB

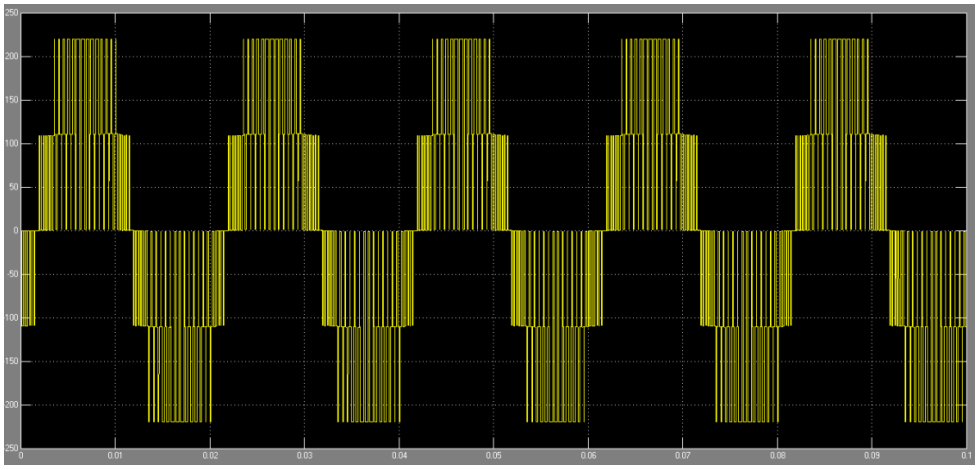

Fig. 10. Output waveform for SPWM

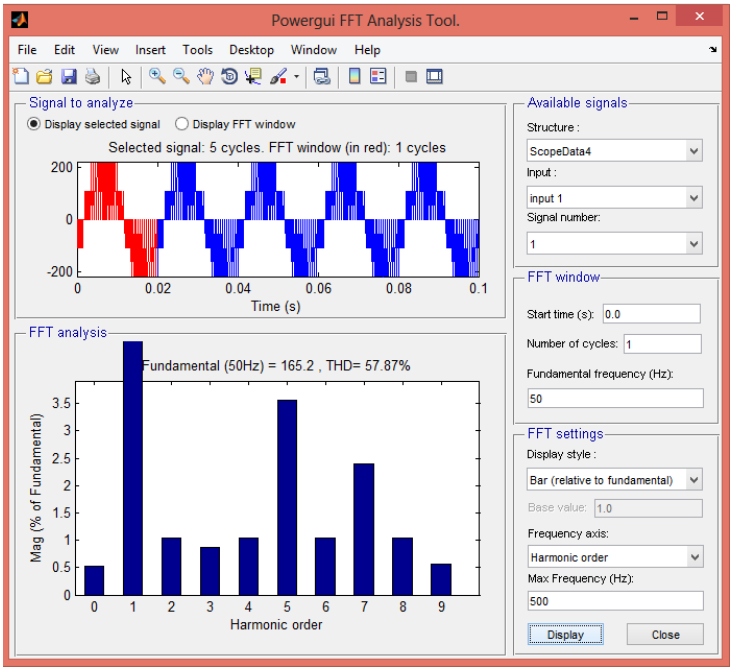

Fig. 11. FFT analysis for SPWM

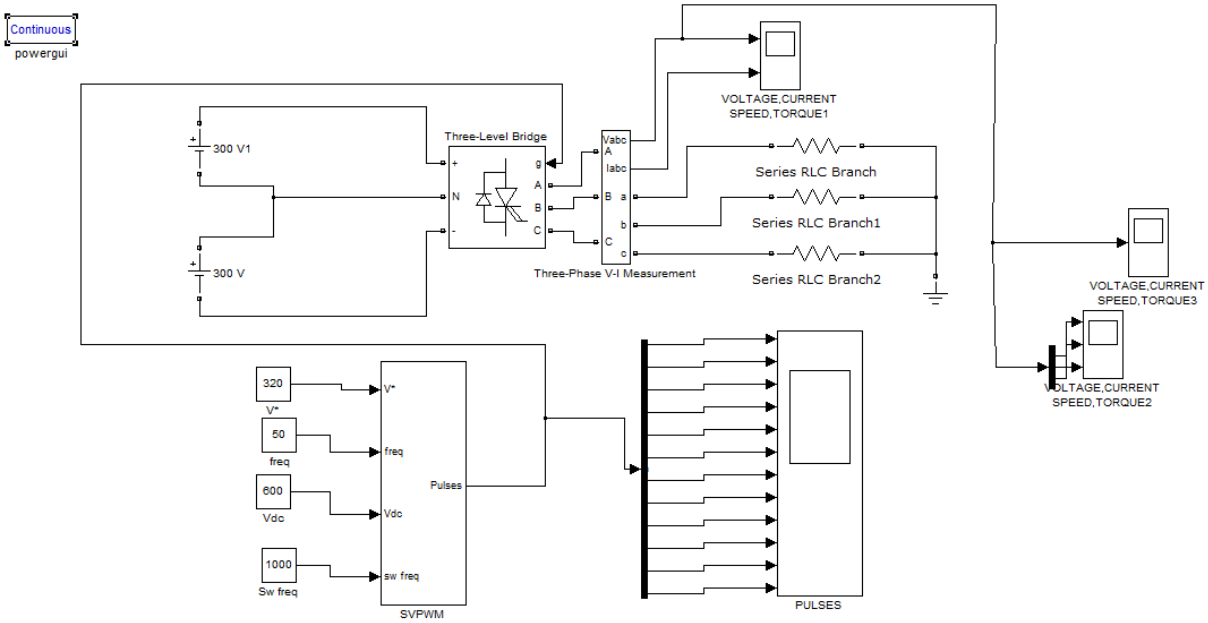

Fig. 12. SVM circuit in MATLAB

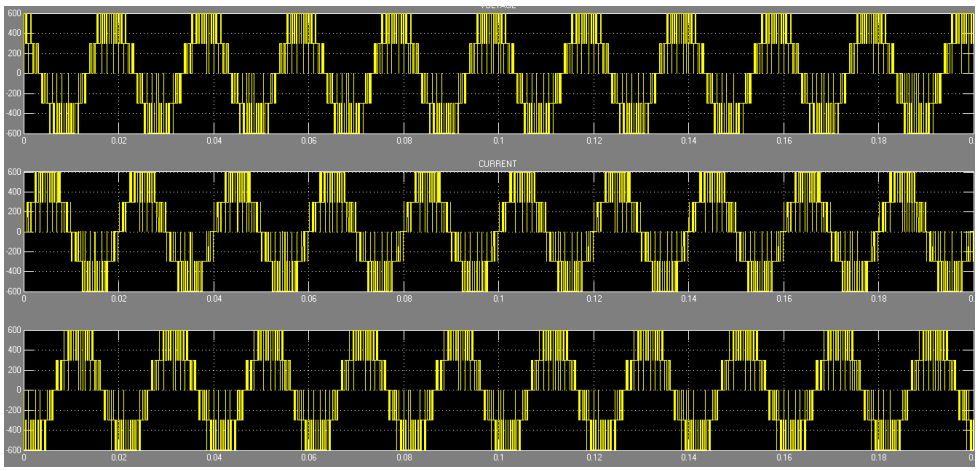

Fig. 13. Output waveform for SVM

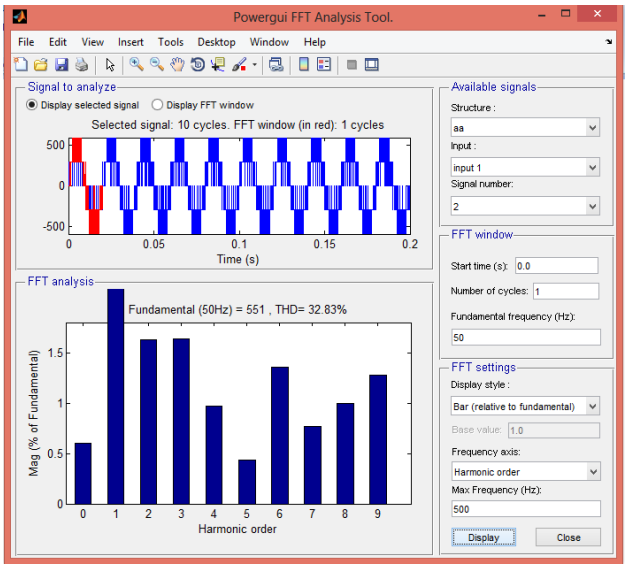

Fig. 14. FFT analysis for SVM

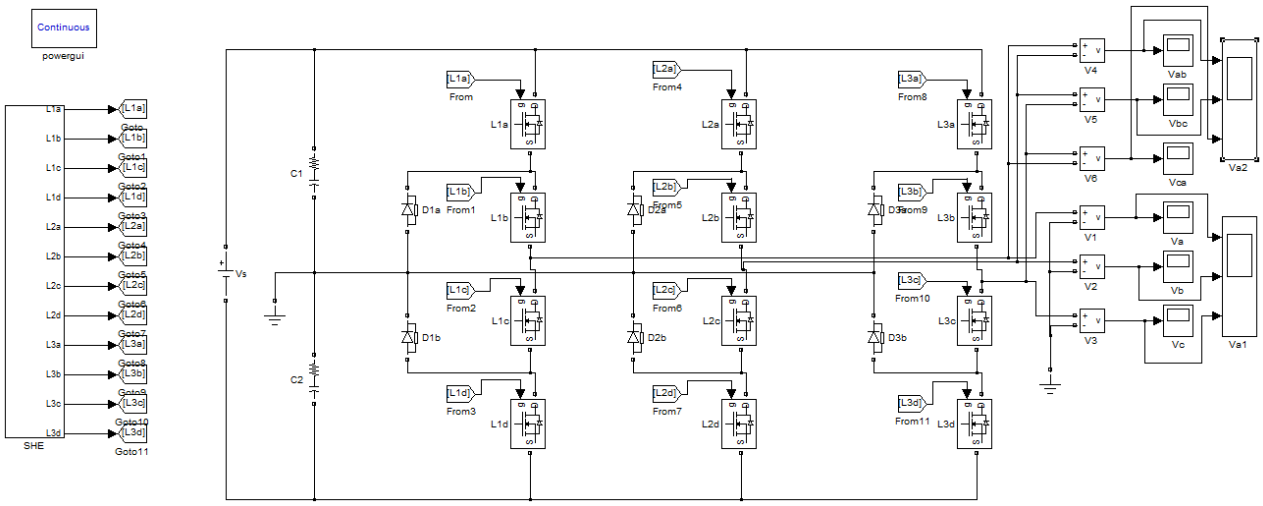

Fig. 15. SHE circuit in MATLAB

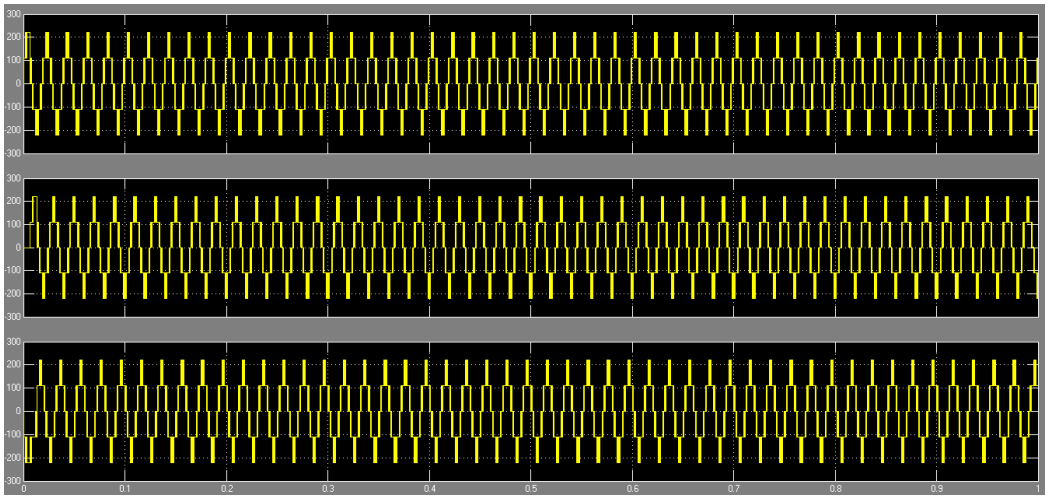

Fig. 16. Output waveform for SHE

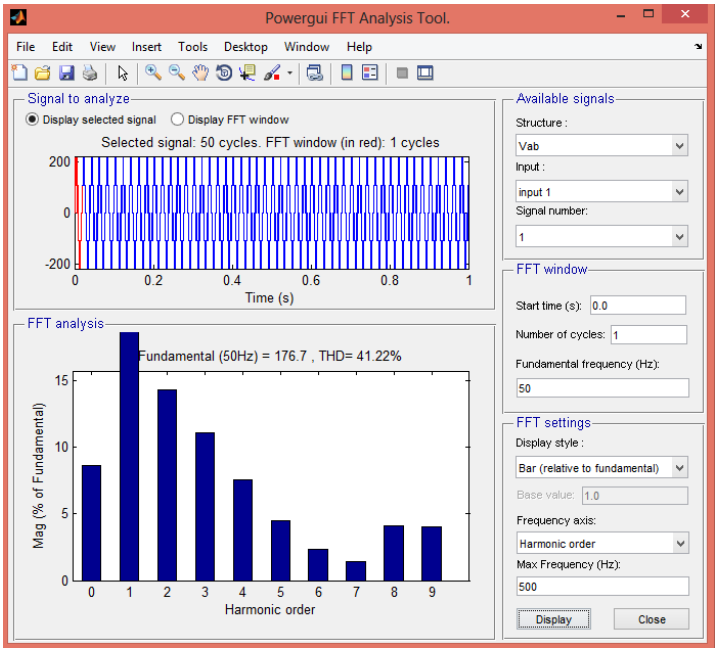

Fig. 17. FFT analysis for SHE

By comparing this three type of modulation techniques based on the THD value we can estimate in which type of modulation the maximum input voltage used. We got less THD in SVM technique and more THD in the SPWM technique. The harmonic content is less in SVM and more in SPWM. It is shown in the below Figure 18.

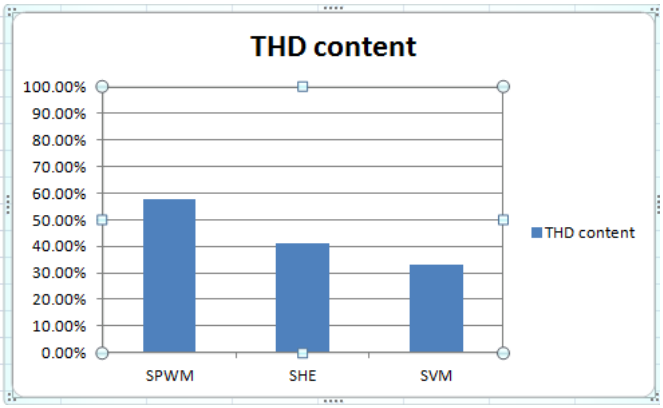

Fig. 18. Comparison of different modulation techniques

7. Conclusion

- A Diode Clamped Multilevel inverter is controlled by different PWM techniques.
- Multilevel converters have matured from being a rising technology to a well-established and enticing answer for medium-voltage high-voltage applications.
- Three topologies and a number of other modulation way shave found industrial application. Initially, the upper power rates in conjunction with the improved power quality are the main market drive and trigger for analysis and development of structure converters.
- However, the continuous development of technology and the evolution of industrial applications will open new challenges and opportunities that could motivate further improvements to multilevel converter technology.

8. References

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